SSPAs with European GaN Devices
Final Report

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CONTRACT REPORT
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ABSTRACT

GaN technology represents a fundamental technological breakthrough for power amplification at microwave frequencies for satellite payload. The introduction of GaN transistors in the new generation of SSPA equipment is significantly improving several performances :

- At electrical level : higher power density, better efficiency, improved robustness, EPC with high voltage value
- At thermal level : higher operational temperature
- At mechanical level : mass reduction, size reduction thanks to higher power density and reduced HPA module number.

Regarding this ARTES 5.1 study, the main conducted activities allowed to evaluate last improvements on European commercial 0.5µm (GH50) and 0.25µm (GH25) GaN HEMT technologies from United Monolithic Semiconductors Foundry. These two GaN technologies were developed in the frame of the GREAT² ESA contract. These UMS GaN processes, makes them the good candidates for space applications from L-band to Ku-band.

Main activity was to design, manufacture and test:
· 1 hybrid HPA module (two iterations) at L-band and based on the UMS GH50 technology
· 1 MMIC HPA module at Ku-band and based on the UMS GH25 technology

As prime contractor of the project, **Thales Alenia Space (TAS)** was in charge of the transistor specification and the design, the manufacture and test of the L-band hybrid HPA module (HPA-1) and the Ku-Band MMIC HPA module (HPA-2). Regarding HPA-2, different architectures were studies (Class AB and Doherty)

United Monolithic Semiconductors (UMS), as sub-contractor and European GaAs and GaN foundry, was in charge of the manufacture and on wafer test of the transistors, power bars and HPA MMIC.

Advanced Modelling Computer Aided Design (AMCAD), as sub-contractor, was in charge of the transistor and power-bar characterization for modelling activity. AMCAD will perform the multi-harmonic load pull measurements for the transistor and power-bar validation after the foundry manufacturing.AMCAD was in charge of the transistor cell non-linear modelling.

The Institut de recherche de l'université de Limoges (XLIM), as sub-contractor, was in charge of the transistor thermal analysis and electro thermal non-linear modelling. XLIM was in charge of the power-bar non-linear modelling and the determination of the operating classes for the L-band hybrid HPA module design.

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1. SSPA FOR FUTURE SPACEBORNE TELECOM APPLICATIONS

1.1 Survey on the Market Trends for L/S-band Telecom application

In order to identify the optimal target with regard to the market needs, TAS has realized a market trends survey for telecom applications in L/S-band.
This survey has been conducted in collaboration with the Telecom Business Line and the SSPA product line.

Two power amplifier families for L/S-band Telecom market have been identified:

- Mobile Satellite Service (MSS) Market:
  - Considered as market of opportunities with high quantities of SSPAs (GB2, Inmarsat) and Medium power requirements [25W-40W] in CW mode.
  - In 2014, a prediction on the power requirements would be: [50W-60W] in CW mode.
  - Only one hybrid HPA GaN module will be required for the last output stage of the SSPA to fulfil the specifications.
- Fixed Service Satellite (FSS) & Data Relay Market:
  - Considered as stabilized market with limited quantities and high power requirements [25W-85W] in CW mode.
  - In 2014, a prediction on the power requirements would be: [110W-130W] in CW mode.
  - Two to three GaN HPA hybrid modules for the last output stage of the SSPA will be required to fulfil the specifications.

Based on the design of the GH50 hybrid HPA module from WP3100 (baseline design), TAS would be able to address both demands:

- 1x HPA module would be used in the SSPA for the future MSS market.
- 2x HPA modules would be used in the SSPA for the future FSS market.

The introduction of the UMS GaN technology in the future L/S-band SSPA equipments will allow to solve the problem of ITAR restrictions. Thanks to this new GaN SSPA equipment, TAS should increase its market share concerning the L/S-band SSPA for Telecom applications.

To conclude: a 30W multi-carrier L-band SSPA equipment based on a single GaN HPA module is the optimal target with regard to the market need , the RF performance (PAE) and the competitiveness.

1.2 Initial L-Band SSPA equipment analysis based on L-Band GH50 Hybrid HPA module performance

This task has been dedicated to:

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- Provide electrical analysis at equipment level of a L-band SSPA using GaAs and GaN Technologies
  - Three L-band SSPA equipment have been studied:
    - "Globalstar2" (GB2) L/S-band SSPA
    - 30W L/S-band SSPA using 2 GaAs hybrid HPA modules
    - 30W L-band SSPA using a single GaN hybrid HPA module designed in WP3100
  - Based on the previous analysis on 30W L-band SSPA equipments (GaAs and GaN), the following aspects have been quantified:
    - Targets for efficiency improvement
    - Targets for DC power consumption reduction and dissipated power reduction
- Provide a preliminary design at equipment level of these SSPA
  - Preliminary mechanical design has been performed on:
    - A 30W L/S-band SSPA using 2 GaAs hybrid HPA modules
    - A 30W L-band SSPA using a single GaN hybrid HPA module designed in WP3100
  - Based on these mechanical designs, following aspects have been quantified:
    - Targets for mass reduction and impact expected
    - Targets for cost reduction including ease of tuning, reduction of number of modules etc…
- Provide thermal analysis on the L-band SSPA preliminary design using GaN technology. The following aspect has been quantified:
  - Operation at a higher base-plate temperature (e.g. 85 to 100deg for a qualification temperature instead of 65deg as proposed today)
- Identify the critical areas related to the usage of the selected GaN technology.

The synthesis of the RF analysis done on L/S-band SSPAs is presented below.

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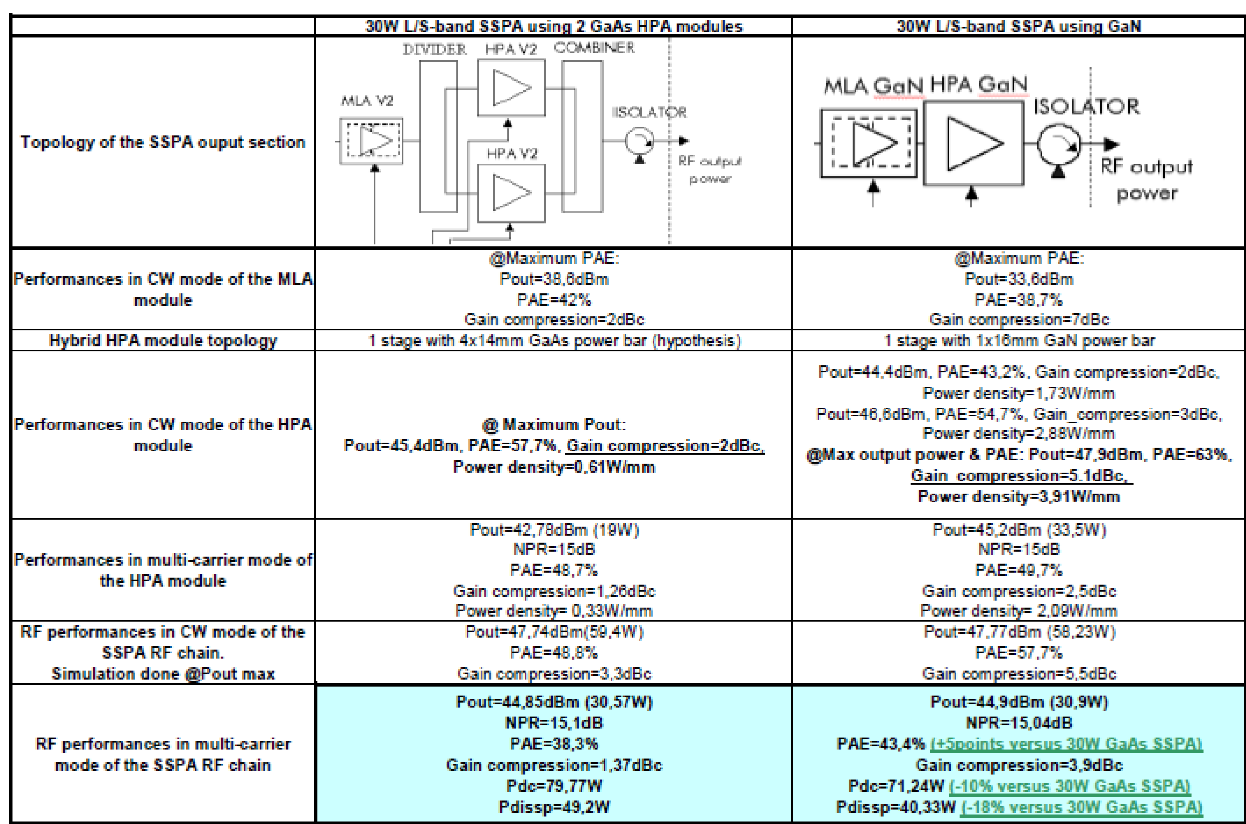

	30W L/S-band SSPA using 2 GaAs HPA modules	30W L/S-band SSPA using GaN
Topology of the SSPA ouput section	DIVIDER, HPA V2, COMBINER, MLA V2, ISOLATOR, HPA V2, RF output power	MLA GaN, HPA GaN, ISOLATOR, RF output power
Performances in CW mode of the MLA module	@Maximum PAE: Pout=38,6dBm PAE=42% Gain compression=2dBc	@Maximum PAE: Pout=33,6dBm PAE=38,7% Gain compression=7dBc
Hybrid HPA module topology	1 stage with 4x14mm GaAs power bar (hypothesis)	1 stage with 1x16mm GaN power bar
Performances in CW mode of the HPA module	@ Maximum Pout: Pout=45,4dBm, PAE=57,7%, Gain compression=2dBc, Power density=0,61W/mm	Pout=44,4dBm, PAE=43,2%, Gain compression=2dBc, Power density=1,73W/mm Pout=46,6dBm, PAE=54,7%, Gain_compression=3dBc, Power density=2,88W/mm @Max output power & PAE: Pout=47,9dBm, PAE=63%, Gain_compression=5.1dBc, Power density=3,91W/mm
Performances in multi-carrier mode of the HPA module	Pout=42,78dBm (19W) NPR=15dB PAE=48,7% Gain compression=1,26dBc Power density= 0,33W/mm	Pout=45,2dBm (33,5W) NPR=15dB PAE=49,7% Gain compression=2,5dBc Power density= 2,09W/mm
RF performances in CW mode of the SSPA RF chain. Simulation done @Pout max	Pout=47,74dBm(59,4W) PAE=48,8% Gain compression=3,3dBc	Pout=47,77dBm (58,23W) PAE=57,7% Gain compression=5,5dBc
RF performances in multi-carrier mode of the SSPA RF chain	Pout=44,85dBm (30,57W) NPR=15,1dB PAE=38,3% Gain compression=1,37dBc Pdc=79,77W Pdissp=49,2W	Pout=44,9dBm (30,9W) NPR=15,04dB PAE=43,4% (+5points versus 30W GaAs SSPA) Gain compression=3,9dBc Pdc=71,24W (-10% versus 30W GaAs SSPA) Pdissp=40,33W (-18% versus 30W GaAs SSPA)

Table 1 : Initial L-band SSPA equipment, RF analysis synthesis

Regarding a future 30W L/S-band SSPA equipment, the preliminary comparison between the two previous GaAs and GaN versions shows important improvements and points to be addressed further:

- Improvement of PAE performance: +5 points
  - Reduction of the number of HPA modules for the last power stage: 2 modules ⇒ 1 module
  - Suppression of combiner losses : 2 ways power combiner (0.3dB losses) ⇒ single HPA module (no loss)
  - PAE_RF_chain_SSPA_GaAs=38%⇒ PAE_RF_chain_SSPA_GaN=43%
- Reduction of the total power consumption and the total dissipated power
  - Pdc: 80W ⇒ 71W (-10%)
  - Pdiss: 49W ⇒ 40W (-18%)
- Increase of the dissipated power at transistor level in the HPA module
  - 0,31W/mm with GaAs technology⇒2,09W/mm with GaN technology
  - Need for an advanced packaging technology
- With a higher baseplate temperature set to +85°C a t equipment level, the GH50 Hybrid HPA module maximum temperature is 160°C
- Increase of the Gain compression level compared to the GaAs SSPA
  - 30W SSPA with 2 GaAs HPA modules: Gain compression=1,4dBc
  - 30W SSPA using GaN: Gain compression=3.9dBc

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- Despite this compression level, the compromise Pout/PAE/linearity remains in favour of the GaN technology in simulation.
- Gain compression has to be confirmed by measurement at power bar level. The gain compression could be reduced by further improvements of the GaN power device technology in the near future.
- Further reliability analysis should demonstrate that this selected operating power (corresponding to the maximum of PAE) remains in the Safe Operating Area of the chosen GaN technology.

- Reduction of HPA module number (2 ⇒ 1) will allow significant improvements at SSPA equipment level in term of size, mass and cost reductions (indeed manufacturing, tuning and assembly phases will be reduced).
  - Footprint reduction : -16%
  - Mass reduction: -20%
  - Cost reduction estimation: -15% in comparison with the 30W L/S-band GaAs SSPA using 2 HPA modules.

This synthesis and the preliminary conclusion are considered as initial and are updated at the end of the study using the measured performance of the developed L-band GaN HPA module. Updated analysis and conclusions (including also comparison with LTWTA equipment) are presented in chapter 4.1

1.3 Survey on the Market Trends for Ku-Band Telecom application

In order to identify the optimal target with regard to the market needs, TAS has realized a market trends survey for applications in Ku-band.
This survey has been conducted in collaboration with the Telecom Business Line and the SSPA product line.
Two markets are identified: TX for TTC and SSPA for Telecom.

- Regarding TX for TTC applications in Ku-band, the main characteristics of the market which is targeted:
  - Required quantity: 8x equipment to be delivered per year
  - Pout>20W in CW mode
- Regarding GaN LC-SSPA for Telecom in Ku-band:
  - Objective would be to replace current LCTWTA solutions
  - Expected quantity: 200x SSPA to be delivered per year
- Regarding satellites constellation for Ku-band internet data application:
  - Pout>20W in CW mode
  - Pout=10W in multi-carrier mode at 15dB
  - Expected quantity: 900x satellites

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1.4 Initial Ku-Band SSPA equipment analysis based on Ku-Band GH25 MMIC HPA module performance

This task has been be dedicated to:

- Identify the topology of a SSPA equipment for the market of active antennas at Ku band
- Provide electrical analysis at equipment level on L-band SSPA using GaAs and GaN Technology
  - Two Ku-band SSPA equipment have been studied:
    - 7W Ku-band SSPA using 2 GaAs hybrid HPA modules (MT-SAT2 equipment)
    - 7W Ku-band SSPA using single GaN hybrid HPA module (GH25 technology)
  - Based on the previous analysis on 7W Ku-band SSPA equipments (GaAs and GaN),following aspects have been quantified:
    - Targets for efficiency improvement
    - Targets for DC power consumption reduction and dissipated power reduction
- Provide a preliminary design at equipment level of Preliminary mechanical design has been realized on:
  - 7W Ku-band SSPA using single GaN hybrid HPA module
  - Based on this preliminary mechanical design and the existing design with GaAs technology ,following aspects have been quantified:
    - Targets for mass reduction and impact expected
    - Targets for cost improvement including ease of tuning, reduction of modules etc…
- Provide thermal analysis on the Ku-band SSPA preliminary design using GaN technology. Following aspects have been quantified:
  - Operations at higher base-plate temperature (e.g. 85 to 100deg for a qualification temperature as opposed to 65deg today)
- Identify the critical areas related to the usage of the selected GaN technologies.

The synthesis of the RF analysis done on Ku-band SSPAs is presented below.

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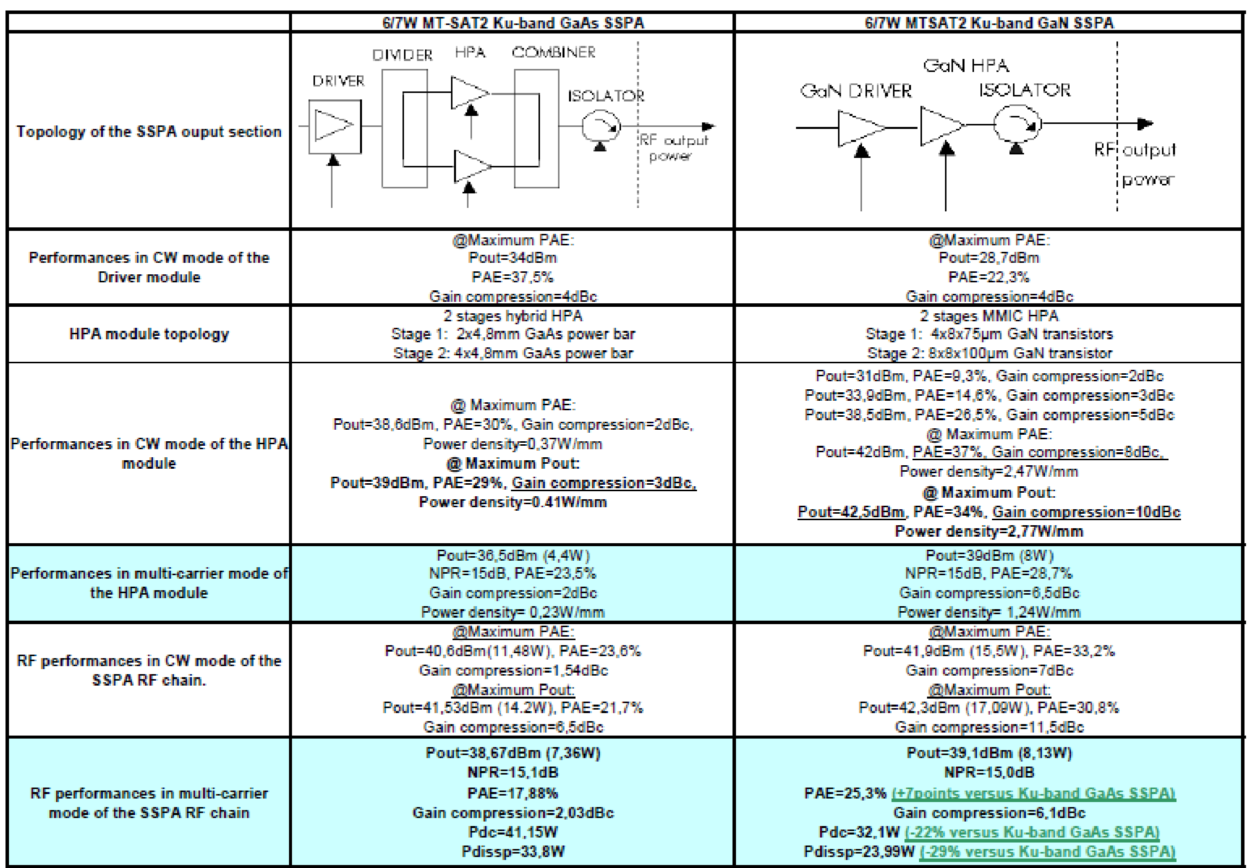

	6/7W MT-SAT2 Ku-band GaAs SSPA	6/7W MTSAT2 Ku-band GaN SSPA
Topology of the SSPA ouput section	DIVIDER HPA COMBINER DRIVER ISOLATOR RF output power	GaN HPA GaN DRIVER ISOLATOR RF output power
Performances in CW mode of the Driver module	@Maximum PAE: Pout=34dBm PAE=37,5% Gain compression=4dBc	@Maximum PAE: Pout=28,7dBm PAE=22,3% Gain compression=4dBc
HPA module topology	2 stages hybrid HPA Stage 1: 2x4,8mm GaAs power bar Stage 2: 4x4,8mm GaAs power bar	2 stages MMIC HPA Stage 1: 4x8x75µm GaN transistors Stage 2: 8x8x100µm GaN transistor
Performances in CW mode of the HPA module	@ Maximum PAE: Pout=38,6dBm, PAE=30%, Gain compression=2dBc, Power density=0,37W/mm **@ Maximum Pout:** **Pout=39dBm, PAE=29%, Gain compression=3dBc,** **Power density=0.41W/mm**	Pout=31dBm, PAE=9,3%, Gain compression=2dBc Pout=33,9dBm, PAE=14,6%, Gain compression=3dBc Pout=38,5dBm, PAE=26,5%, Gain compression=5dBc @ Maximum PAE: Pout=42dBm, PAE=37%, Gain compression=8dBc, Power density=2,47W/mm **@ Maximum Pout:** **Pout=42,5dBm, PAE=34%, Gain compression=10dBc** **Power density=2,77W/mm**
Performances in multi-carrier mode of the HPA module	Pout=36,5dBm (4,4W) NPR=15dB, PAE=23,5% Gain compression=2dBc Power density= 0,23W/mm	Pout=39dBm (8W) NPR=15dB, PAE=28,7% Gain compression=6,5dBc Power density= 1,24W/mm
RF performances in CW mode of the SSPA RF chain.	@Maximum PAE: Pout=40,6dBm(11,48W), PAE=23,6% Gain compression=1,54dBc @Maximum Pout: Pout=41,53dBm (14.2W), PAE=21,7% Gain compression=6,5dBc	@Maximum PAE: Pout=41,9dBm (15,5W), PAE=33,2% Gain compression=7dBc @Maximum Pout: Pout=42,3dBm (17,09W), PAE=30,8% Gain compression=11,5dBc
RF performances in multi-carrier mode of the SSPA RF chain	**Pout=38,67dBm (7,36W)** **NPR=15,1dB** **PAE=17,88%** **Gain compression=2,03dBc** **Pdc=41,15W** **Pdissp=33,8W**	**Pout=39,1dBm (8,13W)** **NPR=15,0dB** **PAE=25,3% (+7points versus Ku-band GaAs SSPA)** **Gain compression=6,1dBc** **Pdc=32,1W (-22% versus Ku-band GaAs SSPA)** **Pdissp=23,99W (-29% versus Ku-band GaAs SSPA)**

Table 2 : Initial Ku-band SSPA equipment, RF analysis synthesis

Regarding a future 7W Ku-band SSPA equipment, the preliminary comparison between the two previous GaAs and GaN versions shows important improvements and points to be addressed further:

- Improvement of PAE performance: +7 points
  - Reduction of the number of HPA modules for the last power stage: 2 modules ⇒ 1 module
  - Suppression of combiner losses : 2 ways power combiner (0.6dB losses) ⇒ single HPA module (no loss)
  - PAE_RF_chain_SSPA_GaAs=18%⇒ PAE_RF_chain_SSPA_GaN=25%
- Reduction of the total power consumption and the total dissipated power:
  - Pdc: 41W ⇒ 32W (-22%)
  - Pdiss: 33,8W ⇒ 24W (-29%)
- Increase of the dissipated power at HPA module level:
  - 13,4W with GaAs HPA module⇒20,2W with GaN HPA module
  - Need for an advanced packaging technology
- Increase of the Gain compression level compared to the GaAs SSPA
  - 7W Ku-band SSPA with 2 GaAs HPA modules: Gain compression=2dBc
  - 7W Ku-band SSPA using GaN: Gain compression=6,1dBc

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  - o Despite this compression level, the compromise Pout/PAE/linearity remains in favour of the GaN technology in simulation.
  - o Gain compression has to be confirmed by measurement at transistor level. The gain compression could be reduced by further improvements of the GaN power device technology in the near future.
  - o Further reliability analysis should demonstrate that this selected operating power (corresponding to the maximum of PAE) remains in the Safe Operating Area of the chosen GaN technology.
- Reduction of HPA module number (2 ⇒ 1) will allow significant improvements at SSPA equipment level in term of size, mass and cost reductions (indeed manufacturing, tuning and assembly phases will be reduced):
  - o Footprint reduction : -28%
  - o Mass reduction: -20%
  - o Cost reduction estimation: -17% in comparison with the 7W Ku-band GaAs SSPA using 2 HPA modules.

This synthesis and the preliminary conclusions are considered as initial and are updated at the end of the study using the measured performance of the developed Ku-band GaN HPA module. Updated analysis and conclusions (including also comparison with LTWTA equipment) are presented in chapter 4.2

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2. DEVELOPMENT OF L-BAND HYBRID GH50 HPA MODULE (HPA-1 MODULE)

This activity is composed of two contractual phases:

- Phase 1 for the first iteration of HPA-1 module (based on 0.5µm process)
- Phase 2 for a second iteration of HPA-1 module (based on 0.5µm process)

Each phases is composed of 5x main activities:

1. A baseline design according to the specified target performances and based on the UMS GH50 characteristics. Using UMS GH50 design kit, load-pull simulations are launched on transistor cell level in order to optimize power bar characteristics (number of transistor cells, total periphery and size of each finger). Thermal analysis on the transistor and the whole structure including the transistor physical description and packaging environment are performed in order to evaluate junction temperature. In order to improve the way to match GaN components, the use of hybrid substrate with high dielectric constant have been considered.
2. The manufacture of the 0.5µm transistors and power-bars (GH50) and the associated on wafer tests.
3. The characterization and modeling of the 0,5µm transistors and power-bars in order to develop an electro-thermal nonlinear model.
4. The detailed design of the hybrid HPA module using electrical transistor and power-bar models from previous activity
5. The manufacture and test of the HPA-1 modules. These tests are carried out in in order to verify if the performance fulfills the requirements defined in the ESA SOW. Multi-carriers RF step stress on 3 hybrid HPA modules manufactured and mounted in test jig are also performed in order to identify the safe operating area related to UMS GH50 process.

2.1 Development of L-band hybrid GH50 HPA module (HPA-1 module): Phase 1

2.1.1 Baseline Design

2.1.1.1 Loadpull simulations

This activity is dedicated to the definition of the HPA-1 baseline design and the transistor level requirements to achieve the following technical performances :

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	L-Band HPA				
Performance within Environmental Requirements	Value	Test condition	C/NC	Proposed value	Comments
Nominal Output power with Multicarrier Signal	>30W	@15dB NPR Worst case over temperature	C		
Power Added Efficiency with Multicarrier Signal	>55%	@15dB NPR Worst case over temperature	-	>45%	
Centre frequency	1.5675 GHz	L-Band	C		
Bandwidth	>50MHz	@ Nominal output power	C		
Gain flatness	+/- 0.25dB	Over the whole BW for fixed input power	C		
Gain with Multicarrier Signal	>16dB	@15dB NPR Worst case over temperature	C		
Gain compression level with Multicarrier Signal	Max. 2dB	@15dB NPR Worst case over temperature		Max. 4dB	@15dB NPR worst case over temperature
Maximum phase shift	<15 deg	From 30dB back-off to 4dB compression	C		
Deviation from linear phase	2 deg pk-pk	versus frequency within BW	C		
Input reflexion coefficient	<-10dB	@ Nominal output power over BW	C		
2nd Harmonic rejection	>30dBc		C		
Main DC voltage supply	>50V		-	40V	Confirmed with UMS
Temperature	-10 deg / +85 deg		C		
Pressure	Ambient and 10e-6 mbar		C		Multipactor free operation will be demonstrated by calculation with a sufficient margin

Table 3 : HPA-1 required performances

The HPA-1 being a low frequency version and the UMS 0.5µm GaN process (GH50) being primarily a discrete transistor process; the HPA-1 is based on hybrid technology.

This study has been achieved by applying the following work philosophy :

- Load pull simulation of elementary transistors. Different sizes and different biasing points have been simulated to find the best possible power added efficiency (PAE), output power trade-off for each transistor size.
- Starting from remarkable load-pull simulations, “VOLTI” analysis have been performed to evaluate NPR performances. Thus, optimum transistor size, biasing point and load impedances at fundamental frequency and up to the 3rd harmonic have been highlighted.
- Power bar size has been chosen to reach the output power performances by direct scaling of an elementary transistor.
- Preliminary design of the HPA has been undertaken. Different materials have been studied to enable optimum input and output matching networks design.
- “VOLTI” analysis have validated the PAE, Pout and NPR trade-off feasibility at HPA level and pointed out the RF performances margin regarding the design risks.

Loadpull simulations have been conducted on two different transistor sizes: 8x250µm and 6x400µm.
Main conclusions about the smith chart analysis for peak PAE performances are:

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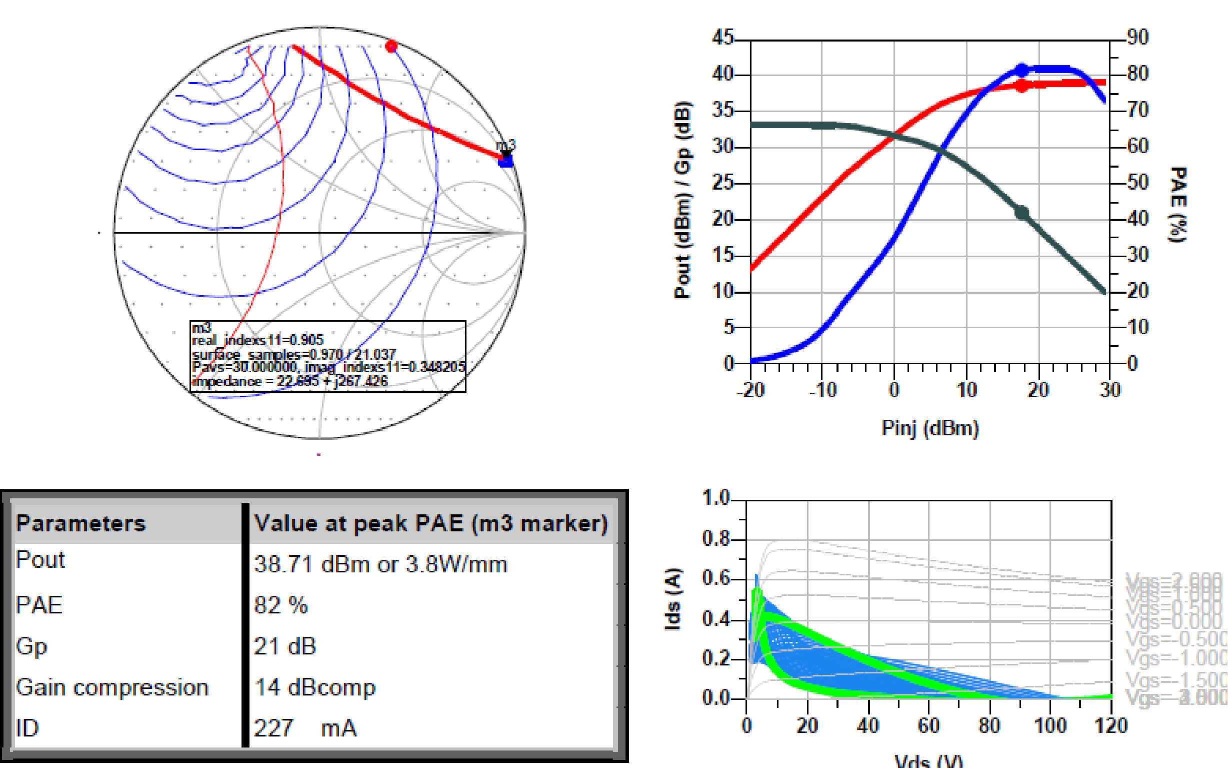
- H2 is very critical for the PAE performance. PAE gradient is high over the whole smith chart and PAE performances can varies from 72% to 43% in the worst case (Zworstcase = 0.97 / 110°). H2 sweet spot impedances is located between Zload 0.97/0° to 0.97/70°. H2 optimization also enables the best output power for PAE peak performance.
- Fine tuning of H1 have to be undertaken in order to maximize PAE performances (+8points PAE) or to find the best trade-off between output power level and PAE.
- H3 allows only a slight improvement of the maximum PAE compared to the re-tuning of H1 with H2 optimized (+2points of PAE). Nevertheless, and even if a wide part of the smith chart is not critical for PAE performances, upper-left side impedances of the smith chart must to be avoided during the design phase because it will lead to a drop of 20 points of PAE in the worst case.
- We notice that PAE peak performance is always correlated to a high level of gain compression around 10dBcomp.



Parameters	Value at peak PAE (m3 marker)
Pout	38.71 dBm or 3.8W/mm
PAE	82 %
Gp	21 dB
Gain compression	14 dBcomp
ID	227 mA

Figure 1 : LP simulation (8x250µm). Third harmonic load impedance optimization for ZL(H1opt) and ZL(H2opt).

A comparison between the 8x250µm and 6x400µm transistor when they are both optimized for maximum PAE up to the 3rd harmonic. A focus is done on output power, power gain and PAE.

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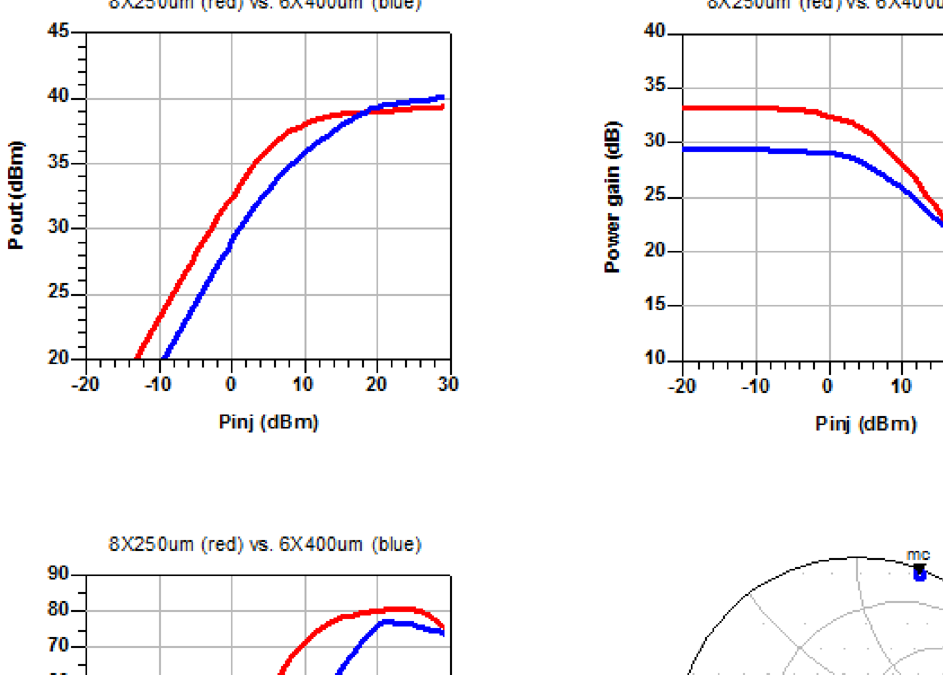

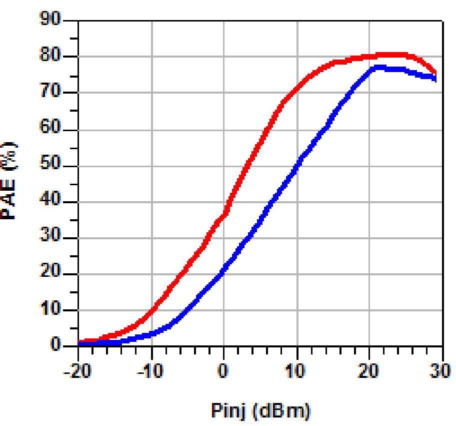

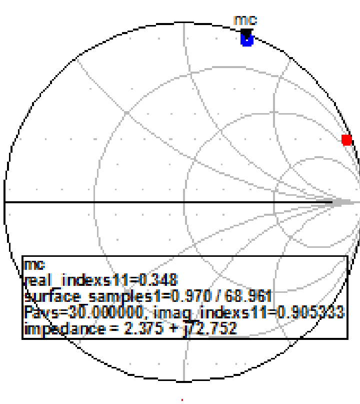

Figure 2 : Comparison between 6x400µm and 8x250µm transistors performances with optimal impedance

As expected, 6x400µm transistor delivers higher output power (Pout > 40dBm) than 8x250µm transistor (Pout = 39dBm) in saturation mode. Moreover, power gain behavior is also coherent with the respective size of the two transistors. In addition, the key point of the comparison is the power added efficiency performances because 8x250µm transistor, in our simulation condition, is far superior to the 6x400µm transistor. It reaches better PAE performances over a wider input power range near the peak PAE than 6x400µm. Finally, when used in back-off mode, PAE is up to 20points better than its competitor. As a consequence, 8x250µm transistor offers the best trade-off for our HPA RF performances requirements where PAE is of primary concern.

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Due to its better PAE performances, the L-Band HPA is based on 8x250µm transistors. Only one stage is necessary regarding the power gain requirements at compression level and the output power performances will be reached using 8 transistors in parallel. Thus, the circuit definition have to be done with UMS 8x8x250µm power bar to matched as close as possible the overall required HPA performances.

2.1.1.2 *Architecture and technologies considerations*

Regarding the elementary transistor cell combination, the 8 transistor power bar (2^n) have been selected. It gives less output power margin regarding the size of the power bar but PAE will be maximized. Moreover, transistor balance is directly linked to the overall HPA stability. This second approach is enhancing PAE by 3 to 5 points.

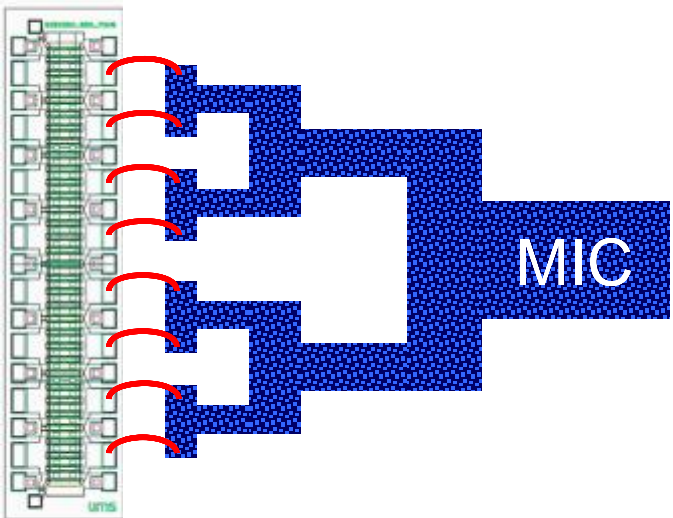

Figure 3 : Power bar considered as macro cell made up of 2n elementary transistor

To design the matching networks, different materials have been evaluated from low to high dielectric constant (Er). See Table Below

Material	Permittivity (εr)	Thickness (µm)	TanD
Al_2O_3	9.9 ±0.2	254	2e-4
OxTi	40	381	
NTK material L	93 ±2	635 / 1016	6.25e-4

Table 4 : Materials table considered for the HPA (input and output network)

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Titanium oxide (OxTi) has been found very suitable for compact design, especially for the input matching network where it gives a balanced trade-off between losses, matching accuracy, and physical dimensions. In a first approach, an input matching network made up of standard microstrip lines model has been implemented in ADS and simulated.
Regarding the output matching network, transistor recombination have been performed as close as possible to the power bar in order to obtain the best possible harmonic symmetry.
Due to the biasing current, a minimum micro-strip line width have to be respected and it implies a careful choice of the material used behind the transistor power bar. In our case, high Er materials are not suitable because it doesn't allow an accurate load impedance synthesis with respect of line width current density constraints.
Thus accurate load impedance synthesis up to the 3rd harmonic as been obtained with Al2O3 material. In a second time, output combiner downsizing was realized by the use of OxTi material to enable its integration in L40 package. As a consequence, the second part of the output combiner has been replaced with OxTi material as shown on figure below.

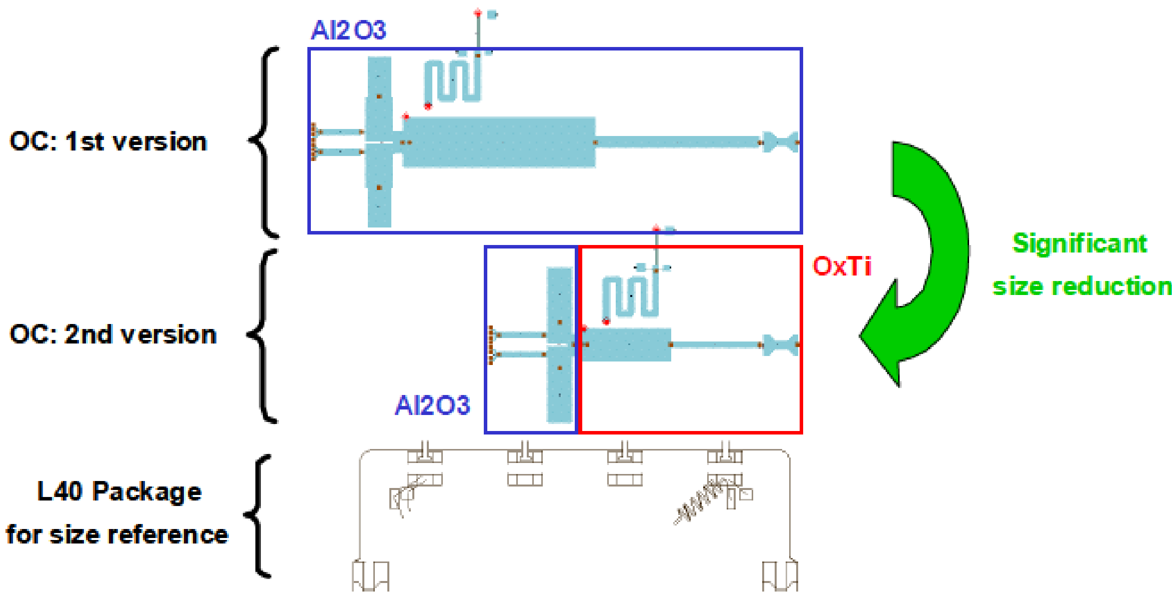

Figure 4 : Output network schematic (Momentum) of the L-band hybrid HPA

2.1.1.3 RF performance

The main RF performances obtained, output power, PAE and power gain are presented below versus input power and versus frequency :

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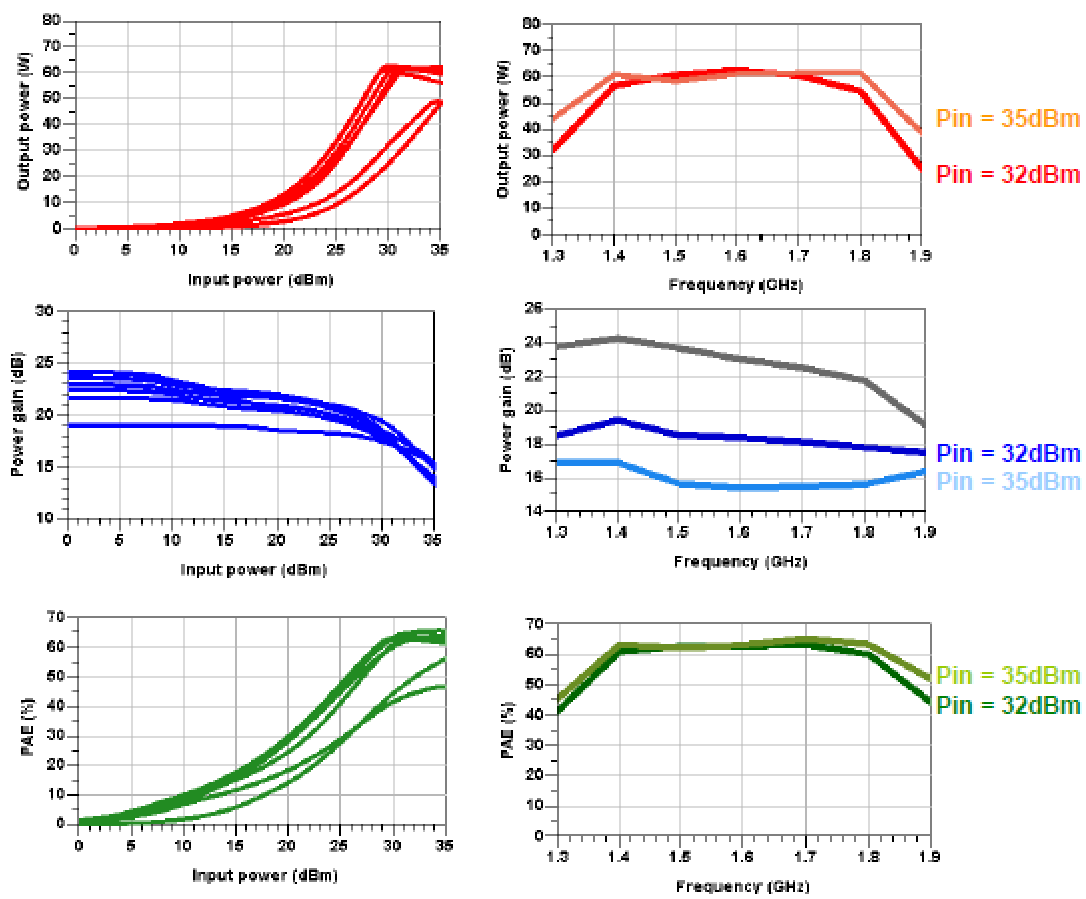

Figure 5 : HPA-1 Module. Baseline Design. HPA RF performances. Pout(W), PAE(%), Gain(dB) versus input power (dBm) and Frequency(GHz).

The frequency bandwidth reaches 400MHz for a centre frequency of 1.6GHz (25% of relative bandwidth). The maximum overall power added efficiency varies from 60 to 65% and is associated to an output power of 60W. It corresponds to a Pout = 4W/mm in saturation mode.

Finally, a Volti analysis has been done at HPA level to check the feasibility of the PAE, output power, NPR trade-off with a multi-carrier signal. On figure below, PAE, NPR and gain compression are drawn versus output power.

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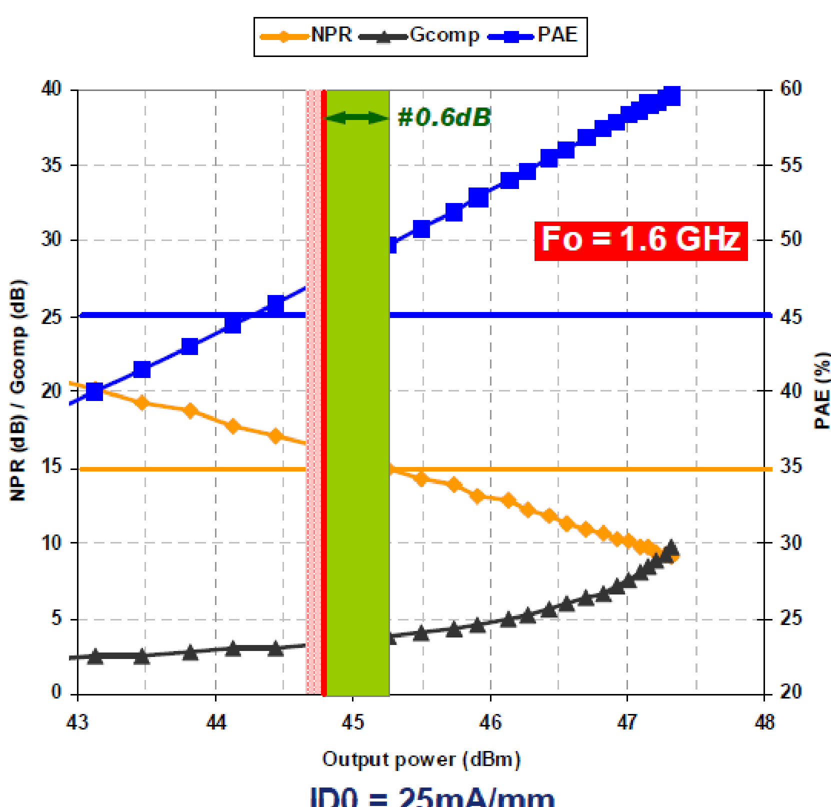

Figure 6 : HPA-1 module. Preliminary GH50 hybrid HPA simulation results in multi-carrier mode. PAE(%), NPR(dB), Gain compression(dB) versus output power(dBm)

As shown below, with an hybrid HPA based on a 8x8x250µm power bar there is very few margin to match both output power, power added efficiency and NPR specifications. So ,different backup solutions, with different power bar setup have been also considered. Table below summarizes these different solutions.

POWER BAR SIZE	GATE LENGTH DEV.	ΔPOUT	PRIORITY	COMMENTARY
8x8x250µm	16 mm	0 dB	+++	
8x8x300µm	19.6 mm	+0.8dB	++	
2x8x8x250µm	32 mm	+3dB	+	2 nominal power bars in // (complex)
10x8x250µm	20 mm	+1dB	-	Not suitable for MMIC design approach
2x8x8x150µm	19,2mm	+0,6dB	-	Complex / high gain

Table 5 : Power bars combinations considered as backup solutions.

2.1.1.4 Packaging solution

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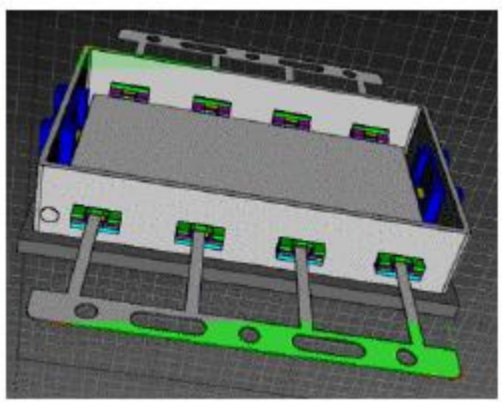
The HPA will be integrated in a L40 power package with MDC (Metal Diamond Composite) base plate.



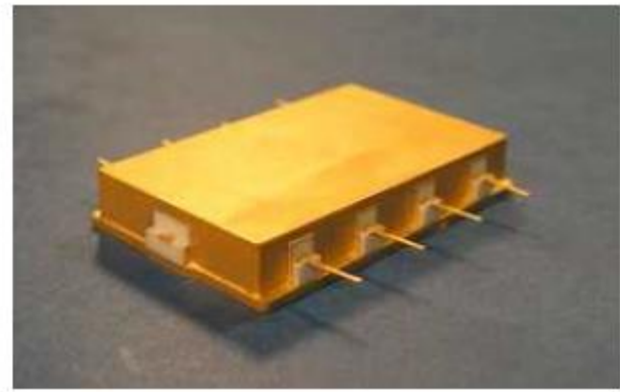


Figure 7 : L40 power package with MDC (Metal Diamond Composite) base plate

This package is space compliant and have been developed by TAS in the frame of the AGAPAC project. Its main characteristics are:

- Able to dissipate up to 100W thermal power (100W dissipated power has been measured in the frame of AGAPAC study where a 36mm power bar has been integrated in this L-band package.
- Overall footprint of the micro-package is set to 20x40 mm.
- Minimized micro-package thermal resistance.
- The L40 package have also been designed taking into account both electrical and mechanical design constraints, multi-pactor and DC current constraints on RF feedthrough.

2.1.1.5 Thermal simulations

Thermal analysis on the transistor and the whole structure including the transistor physical description and packaging environment have been conducted in order to evaluate junction temperature. The thermal behavior of the device represented by a multi-port inputs and outputs SPICE thermal circuit has been generated and used for non-linear modeling activities. These activities are conducted by XLIM.

Thermal simulations are performed with ANSYS software. The job has consisted first to model the transistor structure in 2D and then to extrude it in 3D. The inputs are the geometry of the device: layout and elevations. A very important part of the job is also the mesh of the structure. The knowledge of the thermal properties of materials is also very important. Some materials are considered nonlinear. It is essentially the case for GaN and the SiC substrate which has a significant thickness. Linear thermal properties of the materials are provided below:

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Material	K (W/(m.K)	Cp (J/(Kg.K))	ρ (Kg/m³)
Au	315	130	19320
SiN	35	680	3200
Ni	90	444	8900
AlGaN	40	604	5184
GaN	130	490	6150
AlN	285	600	3230
Diamond Copper	400		
AuSn	58.5		
Al	165		
Glue	2		

Table 6 : Linear thermal properties of the materials

Nonlinear thermal conductivity has been used for thermal simulations. Figure below shows the thermal conductivity of GaN and SiC:

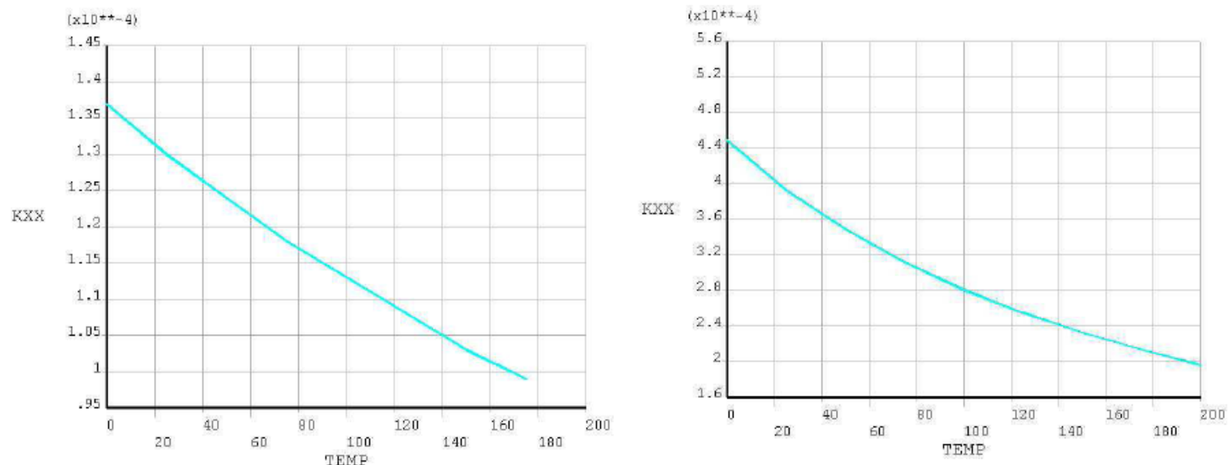

Figure 8 : Non linear thermal conductivity of GaN (left) and SiC (right)

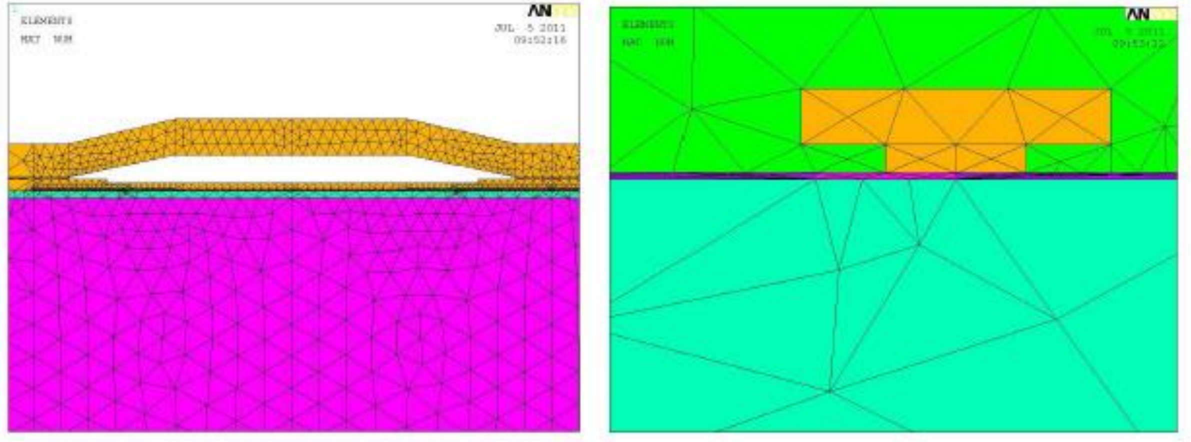

Figure 9 : Cutplane of elementary cell (left)and zoom on the active area (right)

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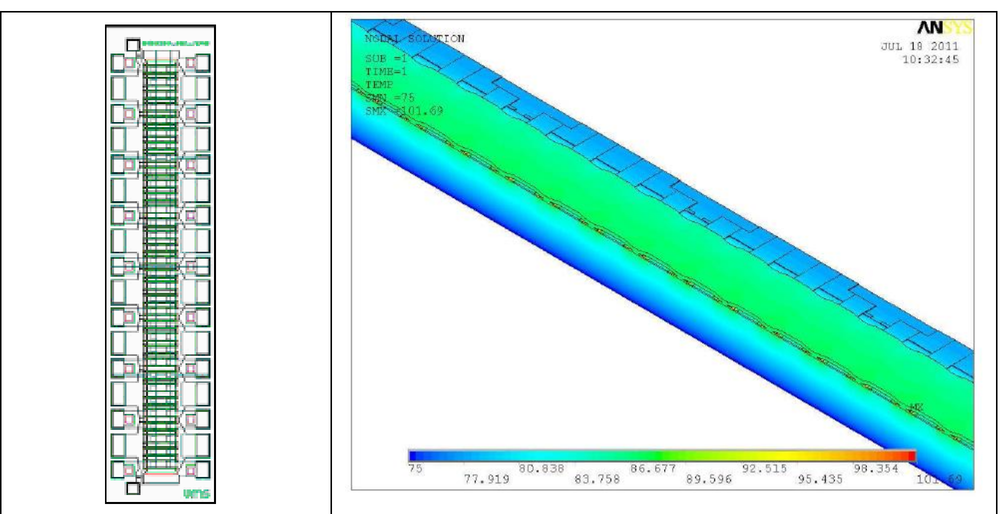

Figure 10 : Temperature profile for Tbase=75°C and 32W of dissipated power

Baseplate\Dissipated Power	28W	32W	36W	40W	44W
50℃	71.87	75.1	78.29	81.55	84.76
75℃	98.28	101.69	105.1	108.58	112
100℃	124.73	128.35	131.98	135.64	139.25
125℃	151	154.78	158.56	162.4	166.16

Table 7 : Maximum Temperature (°C) for various baseplate temperatures and dissipated power

For a power bar build with 8x8x250µm transistor cells, the thermal resistance varies from 6.25°C/W and 7.48°C/W. which is very close to the value obtained for a single elementary cell. This reveals a poor thermal coupling from cell to cell and a quasi-constant temperature along fingers. The third study has been performed to quantify the influence of the packaging. Two different cases have been considered: with or without tab. The first conclusion is that at least 5°C can be gained without tab.
The second one is that the poor thermal conductivity of the glue is clearly a problem. Almost 15°C are lost in this layer. This thermal interface material is not efficient.

To compute the junction temperature of the power bar, the several contributions have been taken into account:
Tcase: 75°C and 36W dissipated power bar. Tab considered

- Tjunction = Tcase + DTcase_to_baseplate + DTbaseplate_to_junction
- DTcase_to_baseplate = 1.286*36 = 46.3°C
- DTbaseplate_to_junction= (0.888+(0.932-0.888)*(121.3-100)/25)*36=33.31°C
- Tjunction = 154.6°C

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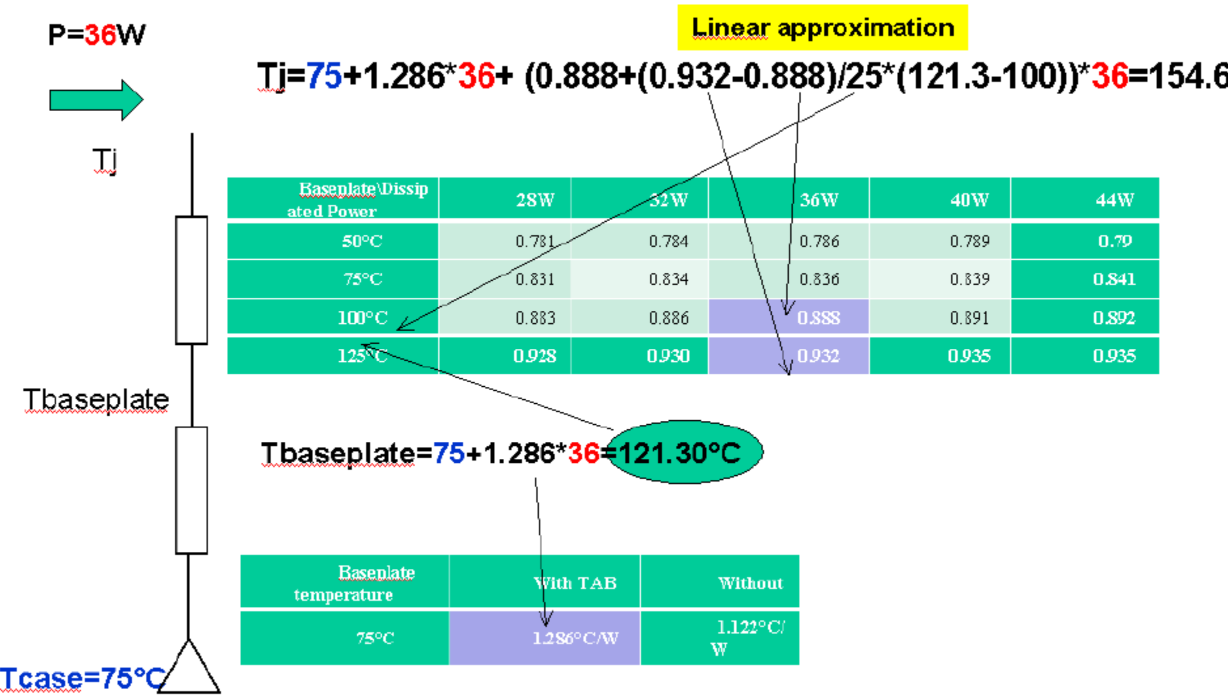

Figure 11 : Temperature calculation for Tcase 75°C 36W dissipated power with tab

Thermal capacitance behavior and equivalent schematic will be implement in the thermal model and include in the modeling report.

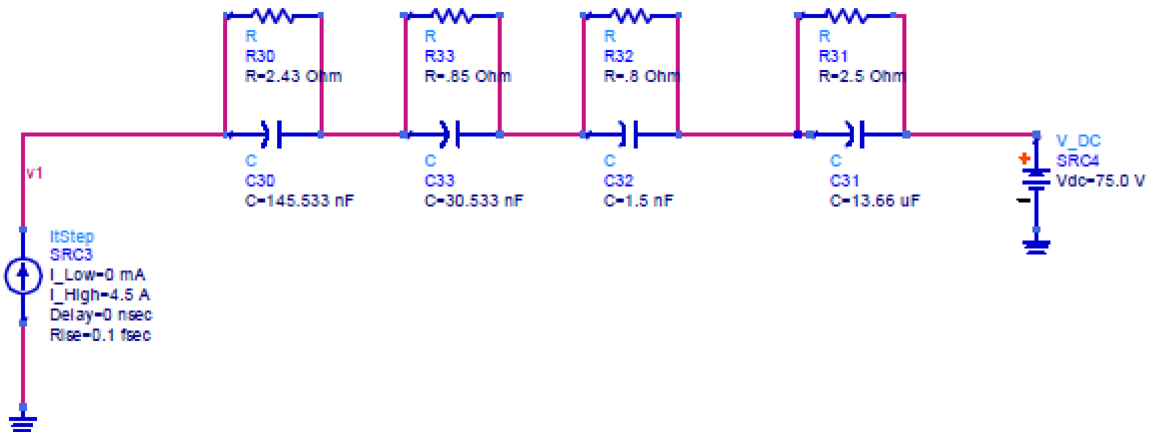

Figure 12 : Preliminary thermal model with 4 cells

2.1.2 Manufacture and test the 0.5µm transistors and power-bars (GH50). Run-1

One specific mask-set called “SABRINA” has been designed, manufactured and tested by UMS. The workflow were as follows :

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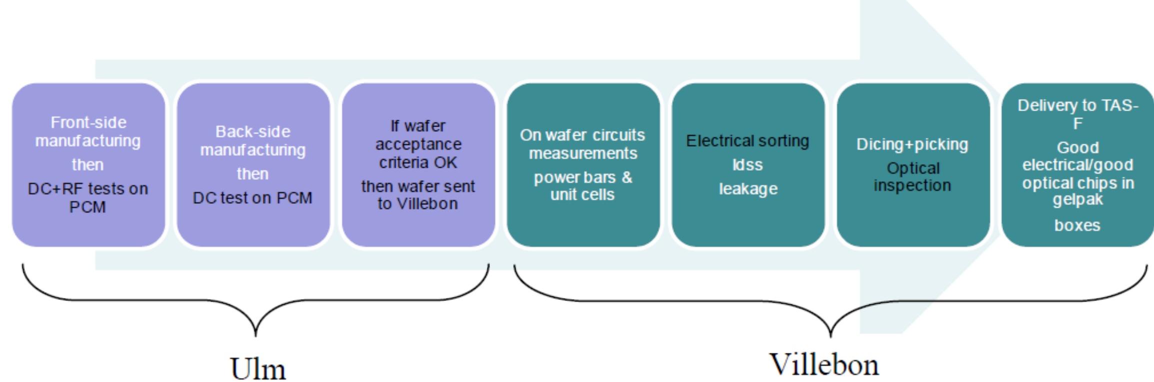

Figure 13 : UMS workflow for the manufacturing and test of GH50 maskset (Run-1)

The PCM tests have shown that the Sabrina wafer 3R034 was in good agreement with the GH50-10 acceptance criteria.

Three power unit cells were included on the Sabrina mask-set :

- 8x150µm
- 8x250µm
- 8x300µm

S parameter measurements were carried out on ten samples located at the center of the wafer. The measurements conditions were as follows:

- Frequency range : 0.5-21GHz
- Frequency step : 250MHz
- Biasing points :Id=50mA/mm Vd=10&40V

For 8x250µm transistor cell, the maximum stable gain /maximum available gain are plotted on the following graph, showing clearly the impact of the biasing conditions as well as the transistor size. A good homogeneity chip to chip is noticed.

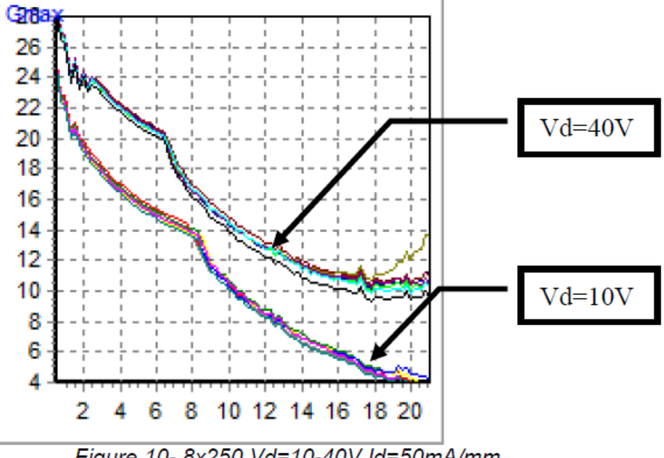

Figure 14 : Run-1 0,5µm wafer manufacturing. Maximum stable gain /maximum available gain for 8x250µm transistor cell

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Four power bars were included on the Sabrina mask-set :

- 8x8x150µm
- 8x8x250µm
- 8x8x300µm
- 10x8x250µm

These Power bars were measured in DC mode thanks to specific probe card. Schottky diode, saturated drain current , pinch-off voltage and gate/drain current leakage were measured on every power bar of the whole wafer. Measured performance of 8x8x250µm power-bar are presented below:

Schottky diode measurements	Wafer mapping: saturated drain current(mA)
Wafer mapping : pinch-off voltage	Wafer mapping : gate leakage in mA at Vgs=-7V&Vds=40V

Figure 15 : Run-1 0,5µm wafer tests. Measured performance of 8x8x250µm power-bar

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In this paragraph, the whole on-wafer tests carried out on the Sabrina wafer(Ref.K514111 3R034) have been depicted. The PCM tests have shown that the Sabrina wafer 3R034 was in good agreement with the GH50-10 acceptance criteria. The power bars tests have enabled to screen the die and to provide good electrical chips to TAS-F. That is also useful to know accurately each power bar for building HPA with chips as close as possible in term of electrical performance.

2.1.3 Characterization and modeling of the 0,5µm transistors and power-bars. Run-1

This paragraph gathers AMCAD Engineering and XLIM tasks achieved within the framework of the ARTES 5.1 SSPAs with European GaN Devices, Phase1 (Run-1). For unitary cell, AMCAD Engineering tasks consisted in pulsed I(V) with pulsed [S] measurements, load pull measurements and devices modeling. For power bar, AMCAD Engineering tasks consisted in load pull measurements. For power bar model, XLIM tasks consisted in the de development and validation of the 8x8x250µm nonlinear electro-thermal model.

2.1.3.1 Unitary cell measurements. Run-1

A pulsed I(V) / RF test bench is used for the measurements. Test bench is described in the figure below.

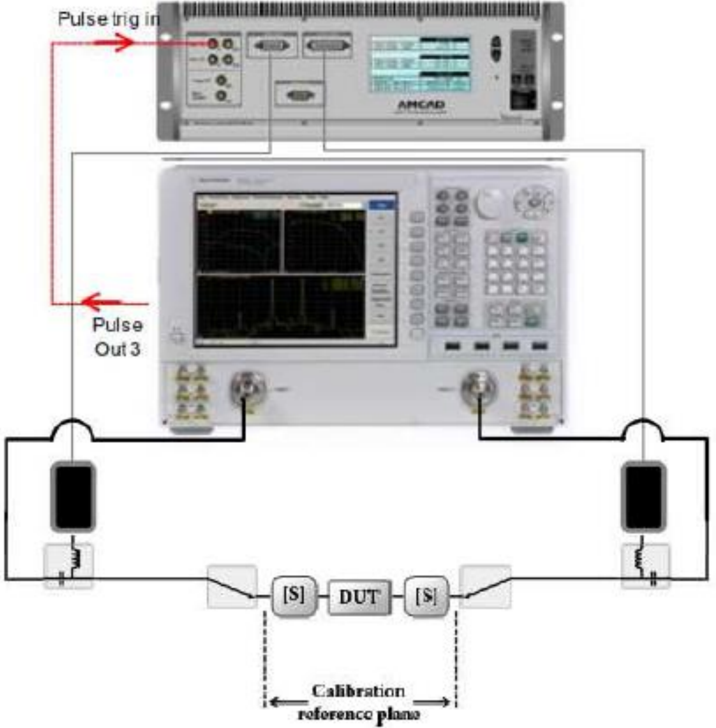

Figure 16 : AMCAD I(V) and [S] test bench for transistors characterizations

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The principle of pulsed measurement is to describe the I(V) network by quasi-isothermal measurements using short pulses around a quiescent bias point selected. The quiescent bias point of rest is provided by the voltage levels and Vgs0 vds0. This results in a current Ids0 polarization. Pulses, whose levels are represented by VGSI, IGSI, VDSI IDSI and describe all the characteristics of input and output of the transistors.

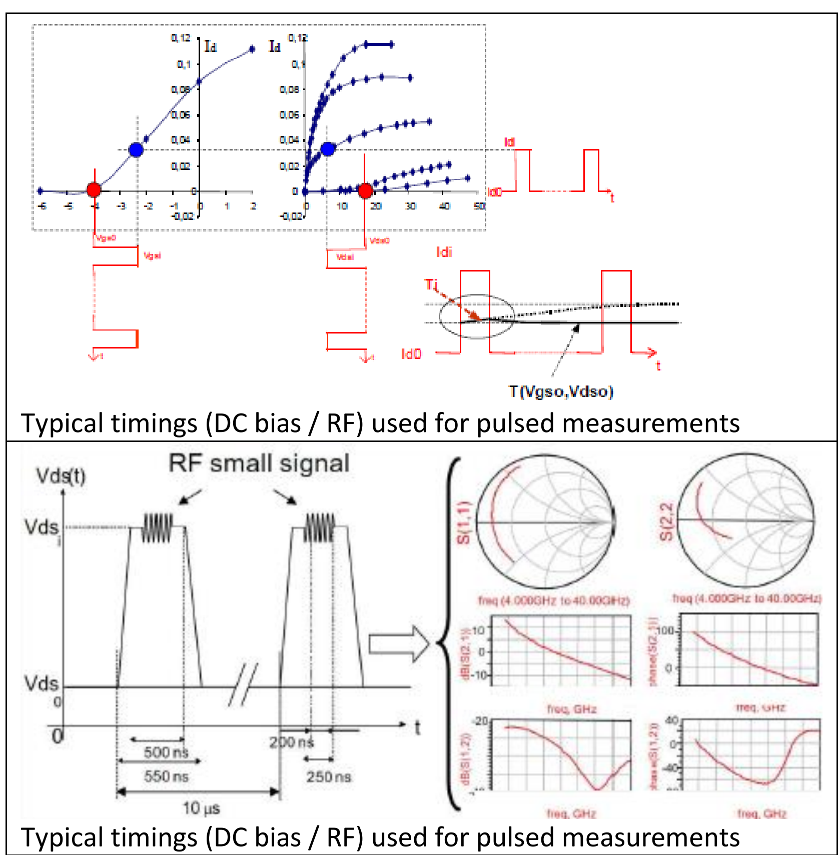

Figure 17 : Principle of the S-parameters measurements in pulse mode

Preliminary pulsed I(V)/RF measurements have been performed on three samples of each topology in order to estimate the process dispersion and to select the most representative samples for the complete characterizations. These dispersive measurements have been performed at ambient temperature (25°C). The results for the different transistor are shown hereafter.

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Figure 18 : Dispersive [S] measurements on transistors 8x250µm GH50 (bias points corresponding to surrounded points on the I(V) curves, Vds=40V)

The representative samples chosen are referred L60. Measurements with temperature have been performed at 25°C, 60°C and 90°C. The results obtained are shown hereafter.

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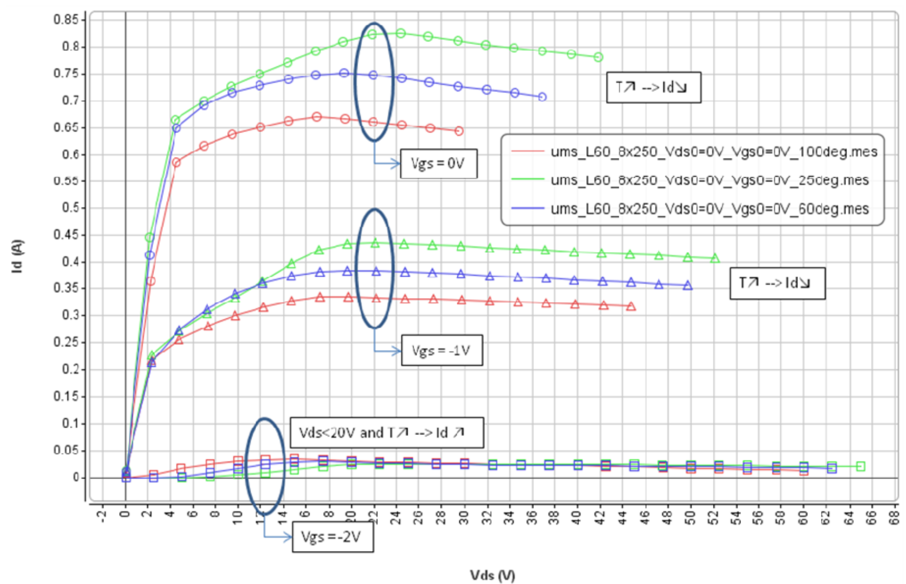

Figure 19 : Output current with different chuck temperature (25°C, 60°C, 100°C) transistor 8x250 L60 measurements

Idss is reduced by 20% to a rise of 75 ° C the chuc k temperature.

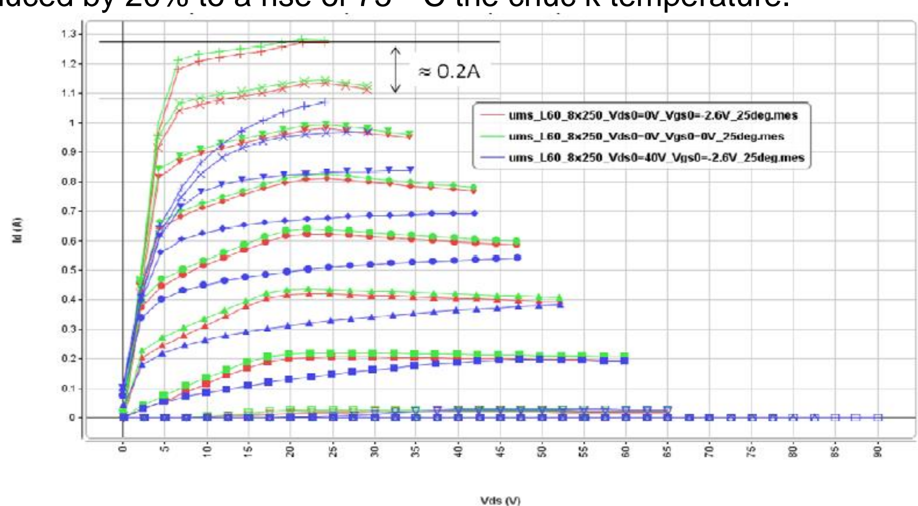

Figure 20 : Highlighted phenomena traps

Only the drain-lag effects are present. The effect on the output characteristic is a reduction of the drain current of 15%. Maximum gain has been plotted for different quiescent bias (40V and Ids from 25mA/mm to 75mA/mm). Example for quiescent bias of 50mA/mm is given below.

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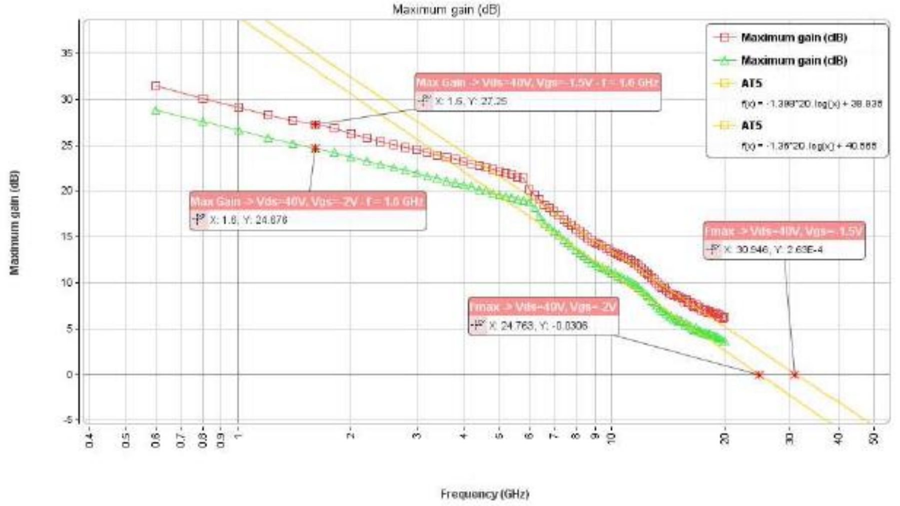

Figure 21 : Maximum Gain @ Vds0=40V, Ids0=50mA/mm

Summary of the unitary cell pulsed i(V) / RF measurements is given in the following table:

Transistor	Dispertion	Idss (A) @ Vds=10V	Max Gain (40V, 50mA)	Fmax (40V, 50mA)
8x250µm L39	✔	0.635		
8x250µm L58	✔	0.632		
8x250µm L60	✔	0.629	24.85dB @ 1.6GHz	24.75 GHz
8x250µm L61	✔	0.621		
8x250µm 061	✔	0.651		

Figure 22 : Summary of the unitary cell – pulsed I(V) / RF Measurements

Load Pull measurements were performed in CW mode at a 1.57GHz. The impedances were optimized at the fundamental frequency and the harmonics 2 and 3. The system set up for the devices characterization is described below.

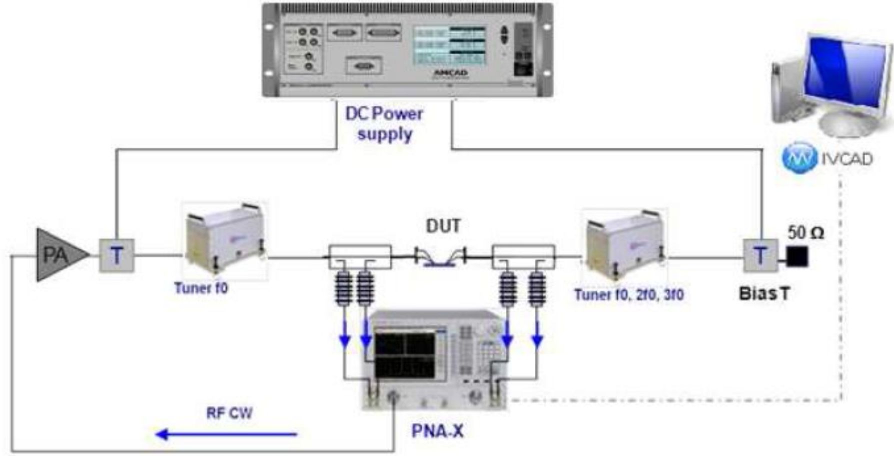

Figure 23 : AMCAD VNA-based load-pull system

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The objective is to find the optimal load impedance added power efficiency (PAE) for f0 = 1.57GHz CW mode. Impedances harmonics 2f0 and 3f0 are also optimized to achieve maximum performance. The 8x250µm component is polarized:

- Vds0=40V, Ids0=50mA (25mA/mm).
- Vds0=40V, Ids0=100mA (50mA/mm).
- Vds0=40V, Ids0=150mA (75mA/mm).

The source tuner is set at 50Ohms. The reference sample is selected transistor L60 (8x250µm), several samples will be used to validate end optimization measures and study the dispersion technology.

The loadpull Optimization methodology used during this campaign is:

- Optimization of f0 load impedance: A first optimization of the load impedance is made at low level to determine the optimal impedance zone when the transistor operates in the linear regime. For this impedance, a power sweep is then performed in order to observe the performance obtained. The power that provides the maximum added power efficiency is raised to perform a second optimization of the load impedance (nonlinear regime). During these optimizations, the load impedances at 2f0 and 3f0 are equal to 50 ohms. During these first measures it appeared that the transistors are conditionally stable, this was confirmed by S-parameter measurements (measurements made on 50Ohms support and source). These Sparameter measurements give a good indication of the places of the Smith chart for which the transistor may be unstable. For biasing point Vd=40V & 25mA/mm, Zload @ f0 = (0.56, 43°), transistor reaches a 64.3% PAE.
- Optimization of 2f0 load impedance: the load impedance at f0 is now set to the optimum impedance PAE. An impedance sweep at 2f0 is now performed to a input power level within the transistor to obtain the maximum PAE. The impedance at 3f0 remains at 50Ohms. For biasing point Vd=40V & 25mA/mm , Zload @ 2f0 = (0.85, 18°), transistor reaches a 71.6% PAE.
- New optimization of the f0 load impedance: with this new optimization of f0 load impedance, the PAE reaches 77.4% (2f0 load impedance is fixed on its optimal and 3f0 is set to 50 Ohms).
- Measurement and Optimization of 3F0: The load impedances at f0 and 2f0 are now set to the optimum impedance PAE. An impedance sweep at 3f0 is now performed to a input power level within the transistor to obtain the maximum PAE. For biasing point Vd=40V & 25mA/mm, Zload @ 3f0 = (0.63, -125°), transistor reaches a 77.2% PAE. With the help of this impedance sweep it’s possible to conclude than 3f0 load impedance do not have a dramatic influence on the PAE performances.

Measured performances are synthesized below:

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Figure 24 : Pout / PAE / Gain vs Pin after loadpull optimization. Optimized load (H1, H2, H3) for optimal PAE performance. Vds=40V, 25mA/mm.

Regarding the RF performance vs Technology Dispersion, the load impedances are substantially similar to the fundamental frequency and harmonic frequency.

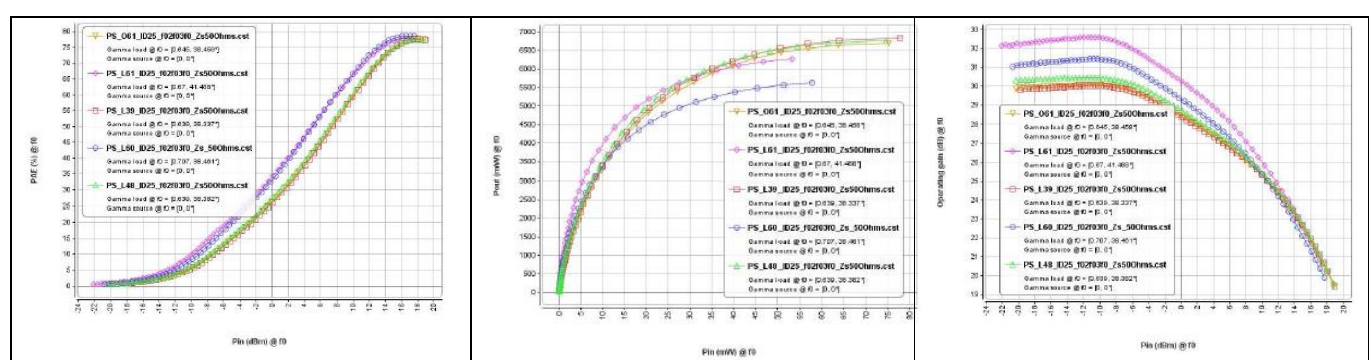

Figure 25 : Loadpull measurements. Performance vs Technology Dispersion. 5x transistor samples tested. 40V, 25mA/mm.

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Tables which summarized the load-pull performance monitored during loadpull measurements on different samples are provided below.

Sample	Linear Gain (dB)	Output Power (W)	PAE max (%)	Zload f0 opt PAE (Ω)	Zload 2f0 opt PAE (Ω)	Zload 3f0 opt PAE (Ω)	Zsource (Ω)
L39	29.7	6.8	77.7	72.9+j97.2	23.3+j115.5	5.9-j5.3	50
L48	30.3	6.7	77.5	72.8+j97.5	23.3+j115.5	5.9-j5.2	50
L60	31.0	5.6	78.8	63.6+j112	24.6+j116.8	5.9-j4.5	50
L61	32.1	6.2	77.8	61.9+j99.6	23.2+j116.5	6.2-j6.3	50
O61	29.8	6.7	77.8	71.9+j98.8	23.7+j116.1	6.0-j5.3	50

Table 8 : Summary of performance monitored during loadpull measurements. Vds=40V and Ids=25mA/mm

Sample	Linear Gain (dB)	Output Power (W)	PAE max (%)	Zload f0 opt PAE (Ω)	Zload 2f0 opt PAE (Ω)	Zload 3f0 opt PAE (Ω)	Zsource (Ω)
L39	29.7	6.9	77.3	77+j97.6	23.2+j115.2	5.9-j5.1	50
L48	30.5	6.7	77	72.9+j97.6	23.2+j115.5	5.9-j5.0	50
L60	31.4	6.0	78.2	63.8+j107.5	25.4+j119.1	6.6-j7.4	50
L61	32.0	6.3	77.3	61.9+j99.7	23.8+j118.2	6.2-j6.1	50
O61	30.2	6.7	77.4	71.8+j98.7	23.3+j114.9	6.0-j5.1	50

Table 9 : Summary of performance monitored during loadpull measurements. Vds=40V and Ids=50mA/mm

Sample	Linear Gain (dB)	Output Power (W)	PAE max (%)	Zload f0 opt PAE (Ω)	Zload 2f0 opt PAE (Ω)	Zload 3f0 opt PAE (Ω)	Zsource (Ω)
L39	29.5	7.0	76.7	72.9+j97.5	23.0+j114.6	5.9-j5.1	50
L48	30.1	6.8	76.3	72.8+j97.6	23.4+j115.7	5.9-j5.0	50
L60	31.6	6.2	77.7	61.4+j103.6	28.5+j133.6	8.3-j9.9	50
L61	31.5	6.2	77.4	61.5+j103.7	28.8+j134.4	8.2-j9.7	50
O61	29.9	6.8	76.8	72+j98.9	23.6+j115.7	6.0-j5.4	50

Table 10 : Summary of performance monitored during loadpull measurements. Vds=40V and Ids=75mA/mm

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2.1.3.2 Unitary cell modeling activity. Run-1

The model provided is a 3 ports transistor model. It is an electro-thermal model. All parameters of the models are available as well as the temperature variable. The model topology is illustrated below.

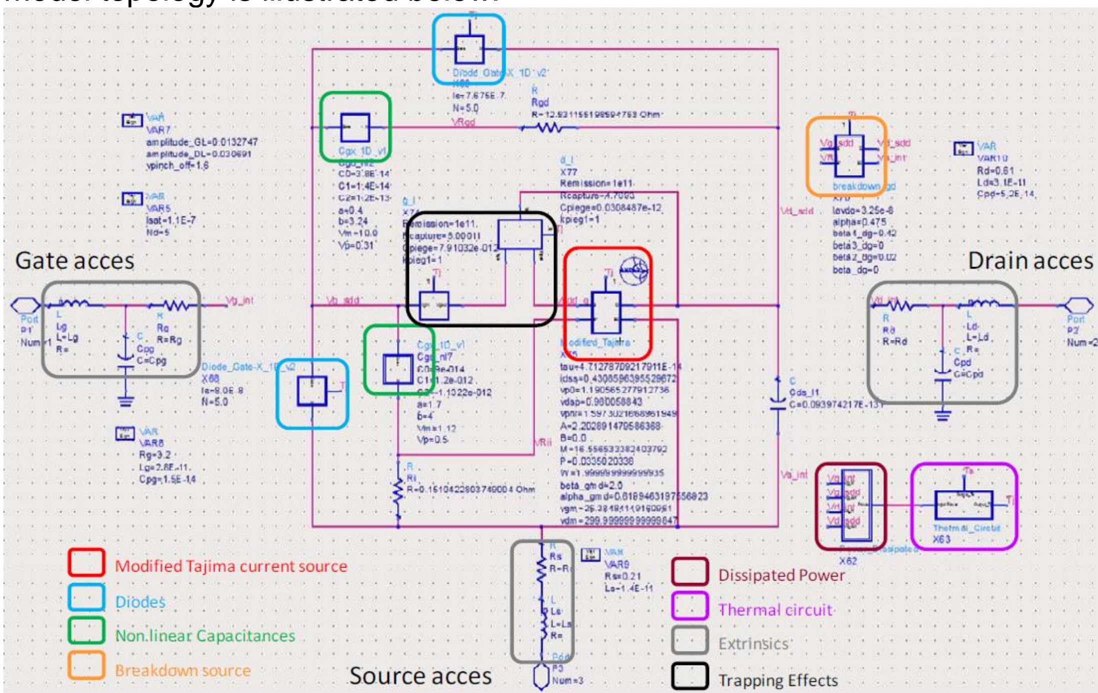

Figure 26 : Elementary transistor cell 8x250µm GH50. Model implemented in ADS

The model adjustment still be a trade-off between all the type of measurements (I(V), [S], load-pull...) and the different operating conditions (bias, temperature, frequency...) in order to have a coherent model. Some comparison (measurements/simulations) are provided below the very good accuracy of the transistor model.

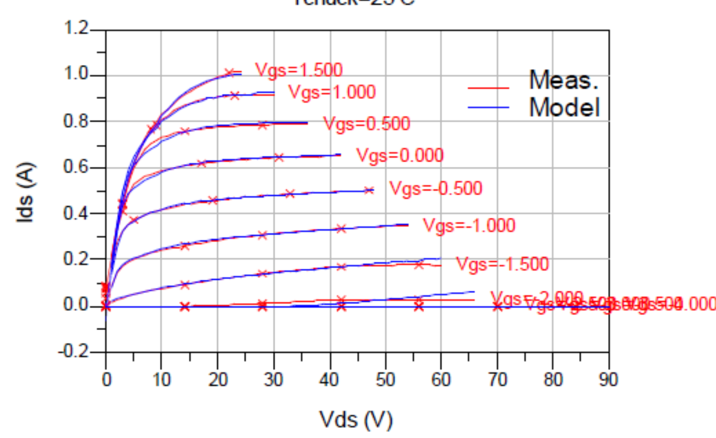

Figure 27 : 8x250µm transistor model validation. I(V) curves comparison. Bias conditions : Vds=40V, Ids0=25mA/mm. Temp=25°C

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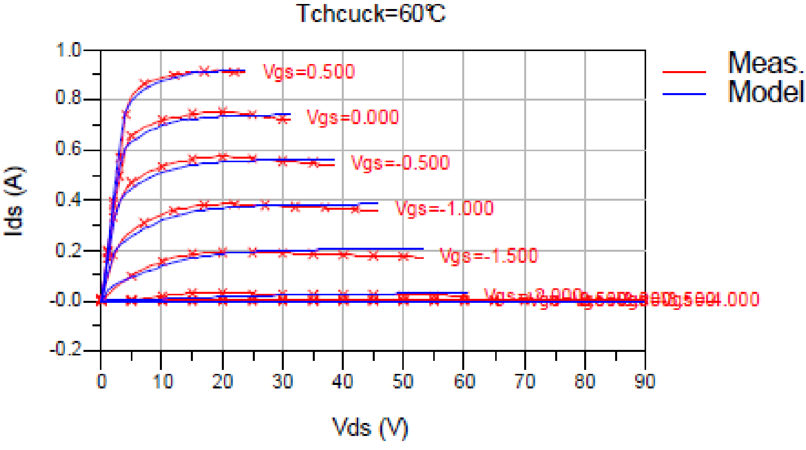

Figure 28 : 8x250µm transistor model validation. I(V) curves comparison. Bias conditions : Vds=0V, Vgs=0V. Temp=60°C

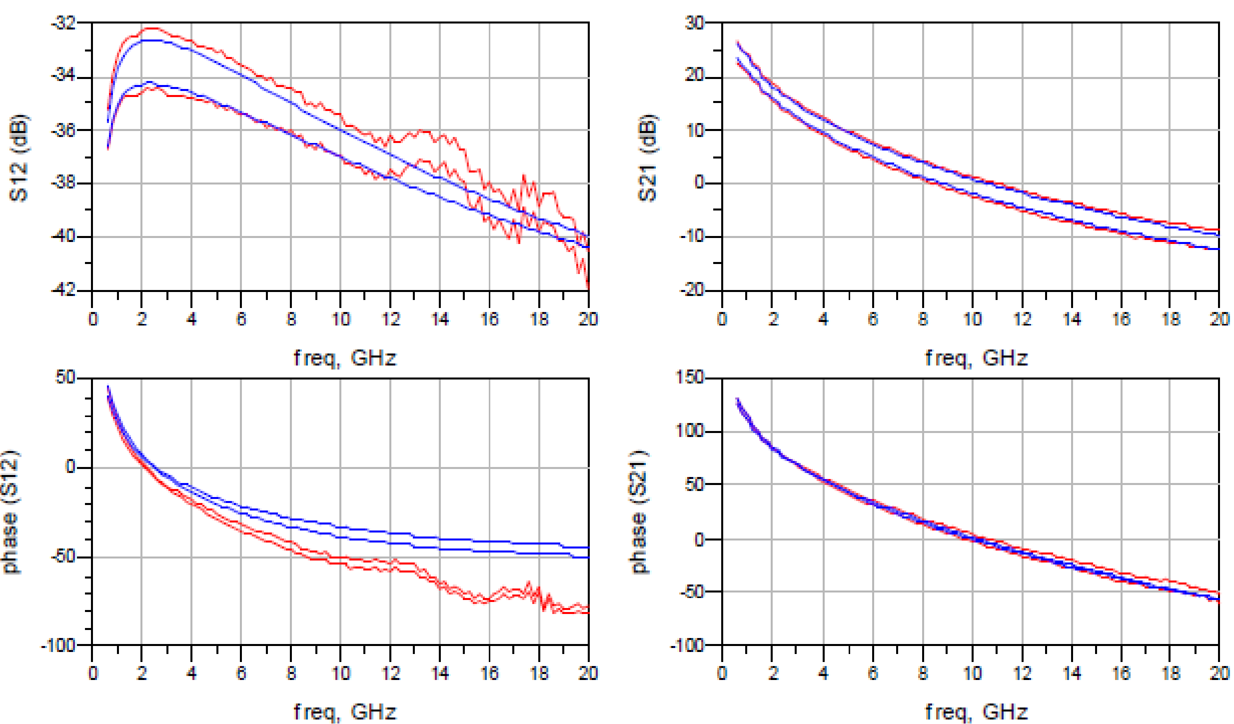

Figure 29 : 8x250µm transistor model validation. [S] parameters comparison. Measurement. vs Model 8x250µm @Vds0=40Vand Ids0=25mA/mm

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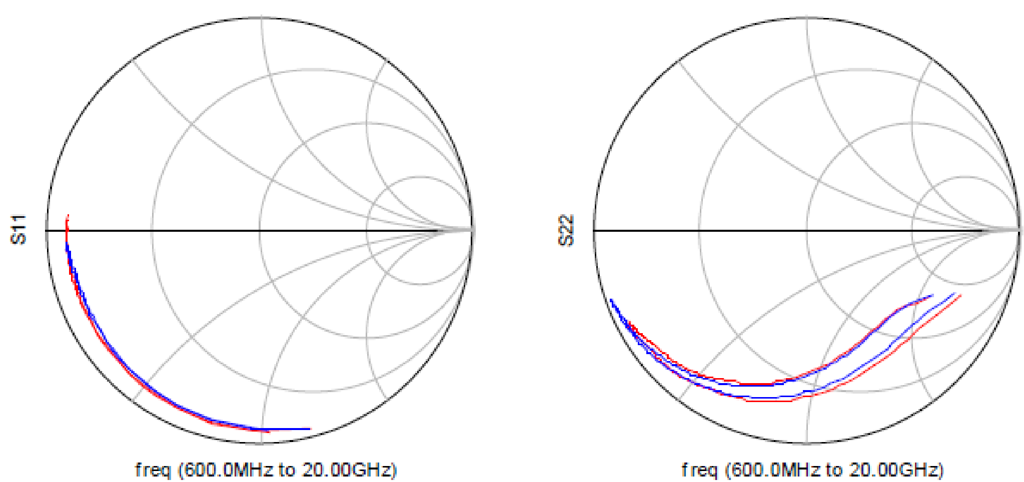

Figure 30 : 8x250µm transistor model validation. [S] parameters comparison. Measurement. vs Model 8x250µm @Vds0=40V and Ids0=25mA/mm

In the load-pull configuration, the comparison is performed at RF_freq=1,57GHz and for several load impedances including the optimum ones.

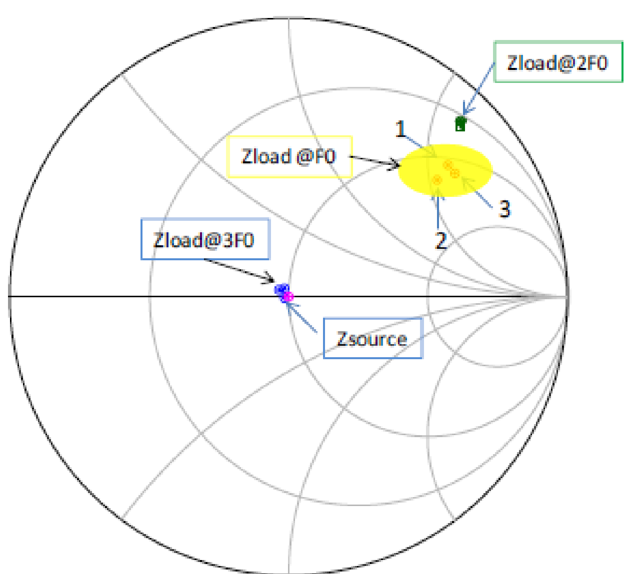

Figure 31 : 8x250µm transistor model validation. Selected impedances used for loadpull simulations/measurements comparison

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Figure 32 : 8x250µm transistor model validation. Loadpull simulations / measurements comparison. Vds0=40Vand Ids0=25mA/mm

2.1.3.3 Power Bar measurements. Run-1

This paragraph sums AMCAD Engineering works achieved on the GaN Power Bar (8x8x250um) provided by Thales Alenia Space: Load-pull measurements PAE optimization (f0, 2f0). The tasks consisted in :

- load-pull measurements to determine the optimum load impedances for the best PAE,
- source impedance is set in order to obtain max Pin.

During the power bar measurements, the operating conditions used are the following:

- RF signal is in pulse mode: F0=1.57 GHz,
- Pulse width=100µs, Duty cycle=5%.

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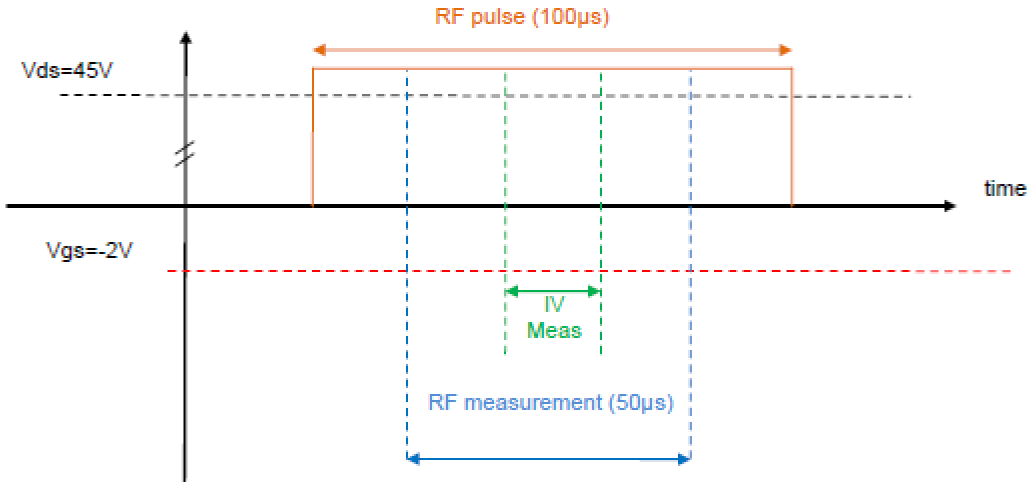

Figure 33 : Measurement chronogram of the Power bar

The Load-pull test bench used during power bar measurement is described below:

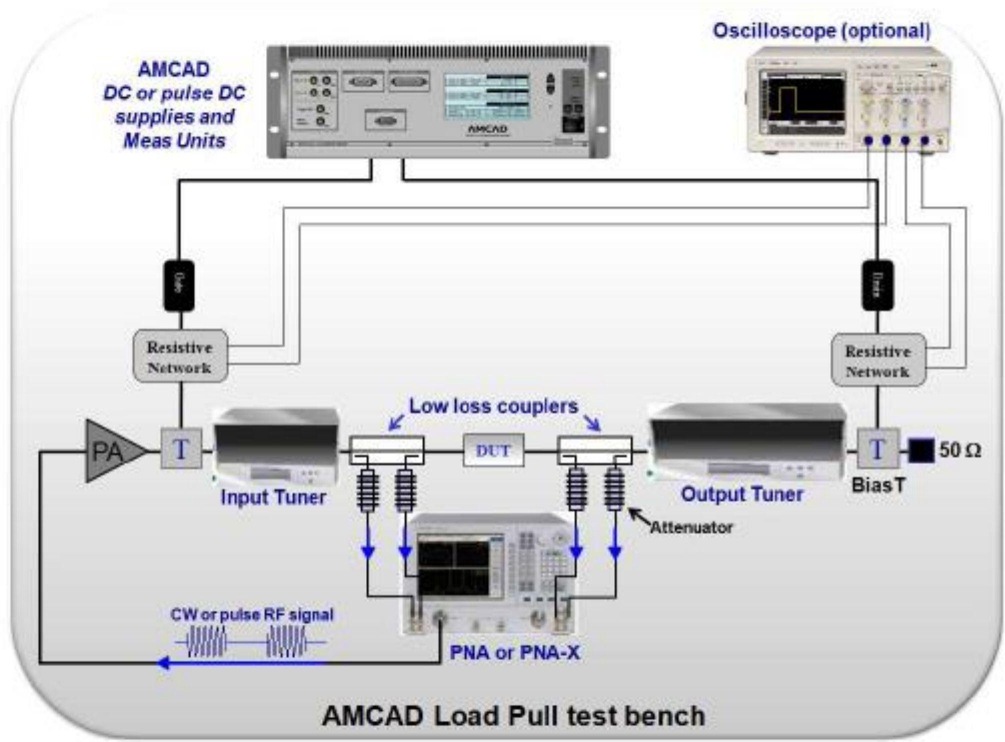

Figure 34 : AMCAD VNA-based load-pull system used for loadpull measurement of power-bar

Two types of measurements are made:

- Direct measurements in the SMA connectors plans
- Measurements in the power bar plans with a de-embedding step

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measurement plans

Power bar test fixture – Measurement plans

Measurement plans

Power bar test fixture – Measurement plans

Figure 35 : Power bar test fixture – two types of measurement plans

In order to provide measurements to the power bar plan a TRL kit has been provided by Thales Alenia Space. From the calibration kit provided, S-parameters files representative of the input circuit (Mic_IN) and output circuit (MIC_Out) of the power bar have been built.

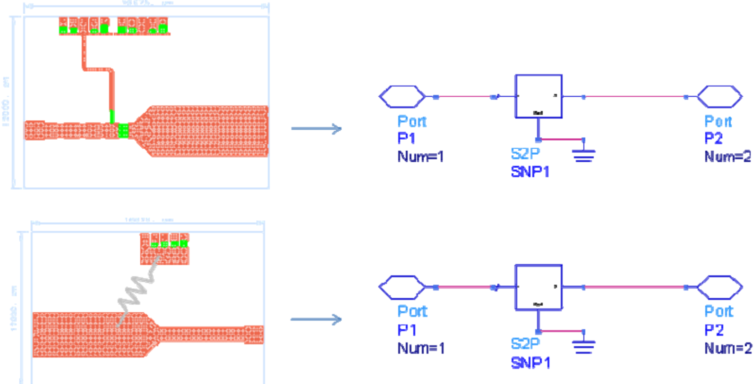

Figure 36 : MIC_In / MIC_Out

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Calibration kit- Line

Calibration kit- Thru

Calibration kit- Open/Short

Calibration kit- Short/Open

Figure 37 : TRL kit

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The power bar characteristics could be defined using measured S-parameters files of the input and output fixture. With the de-embedding files all the performances are transformed.

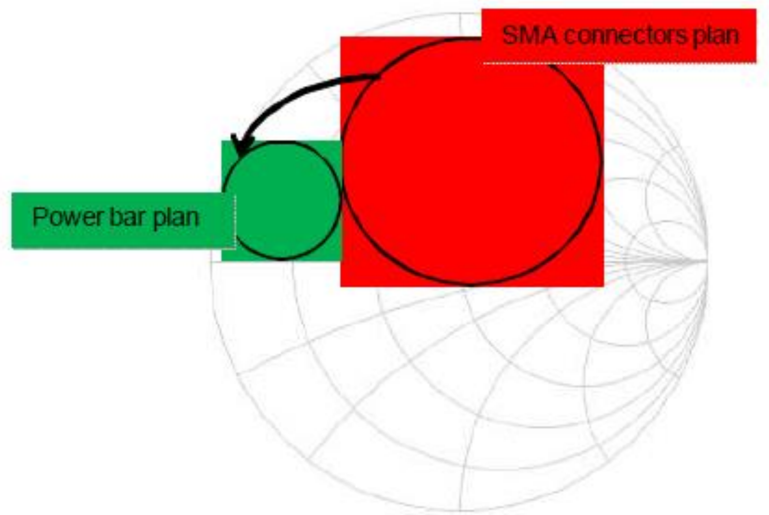

Figure 38 : Example of a load impedance transformation caused by the de-embedding (@F0)

2x power bars have been measured with load-pull test bench under the following conditions

- Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), SMA reference plane, power bar n°4
- Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), SMA reference plane, power bar n°2
- Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), Power Bar reference plane, power bar n°4
- Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), Power Bar reference plane, power bar n°2

For each power bar, the loadpull optimization methodology used during the campaign is:

- First optimization of Zload @ F0(fundamental frequency)
- Optimization of Zload @ 2F0
- New optimization of Zload @ F0 with Zload@2F0 optimized
- Final monitoring of the performance of the power bar for the load impedance (Zload@F0 and Zload@2F0) around the optimum PAE

Performance of the Power bar n°4 monitored in the Power-Bar reference plan are presented below:

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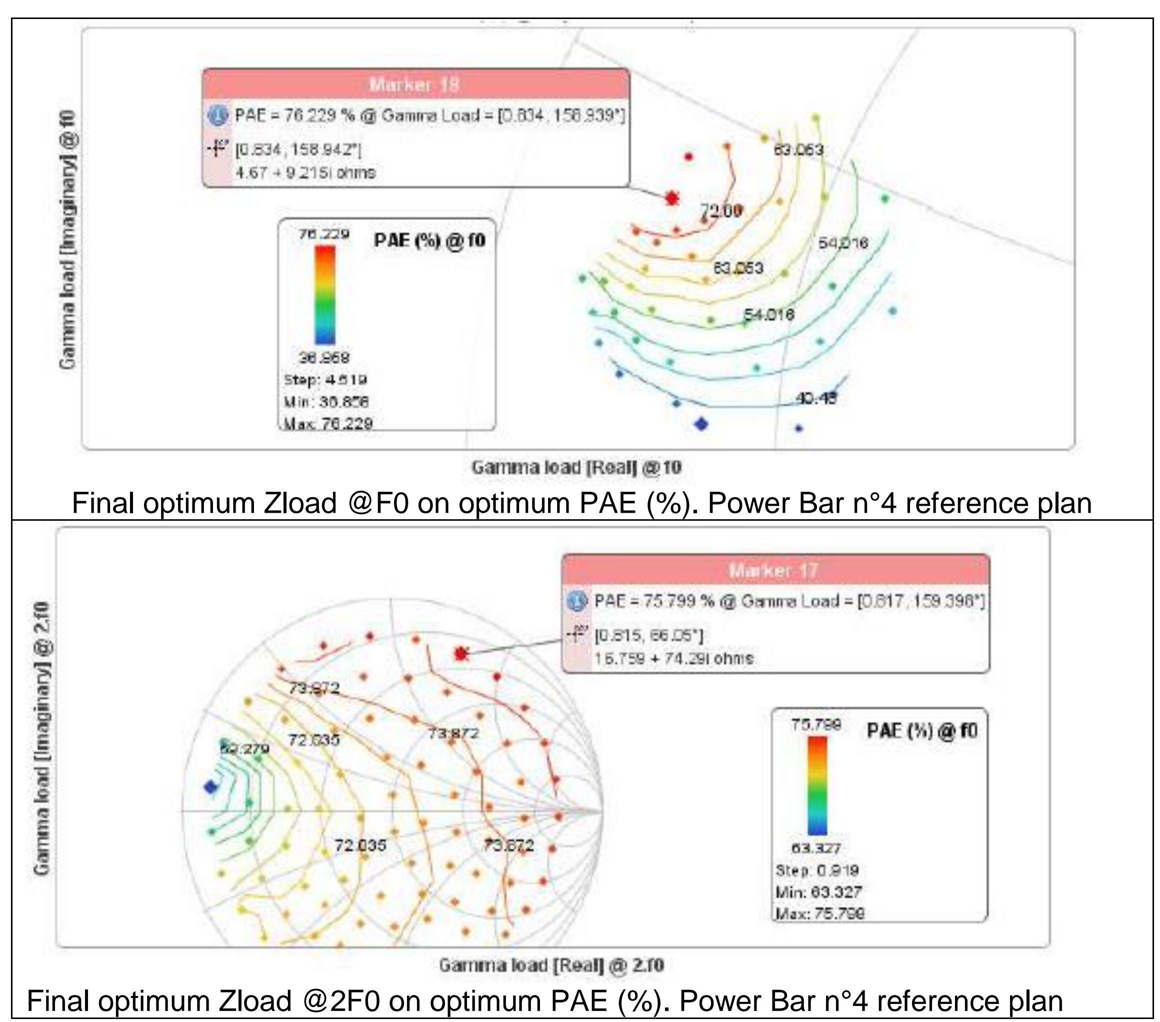

Final optimum Zload @F0 on optimum PAE (%). Power Bar n°4 reference plan

Final optimum Zload @2F0 on optimum PAE (%). Power Bar n°4 reference plan

Figure 39 : Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), Power Bar reference plane, power bar n°4. Optimum Zload @f0 and @2f0

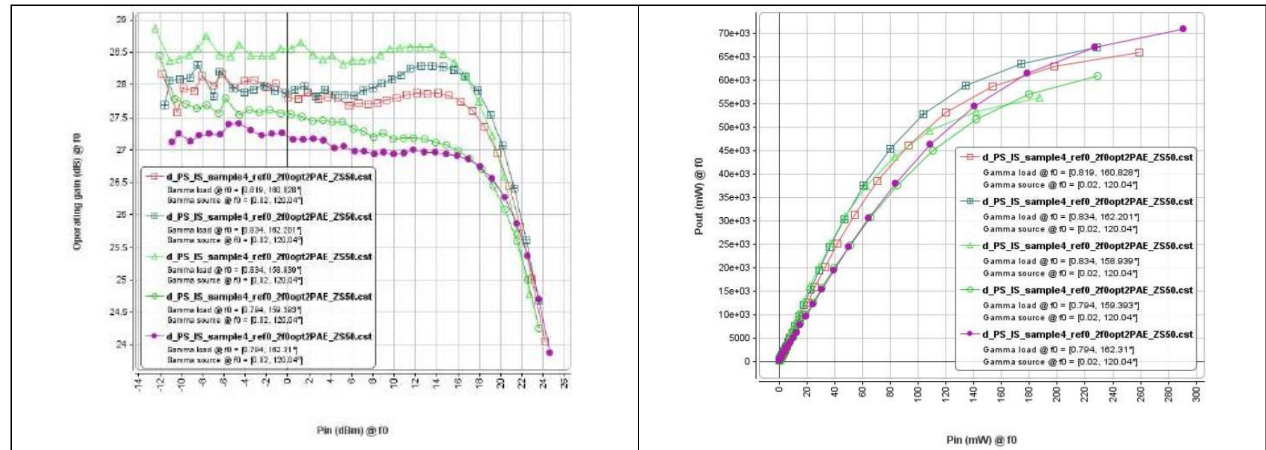

Figure 40 : Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), Power Bar reference plane, power bar n°4. Gain(dB) / Pout(dBm) vs Pin(dBm)

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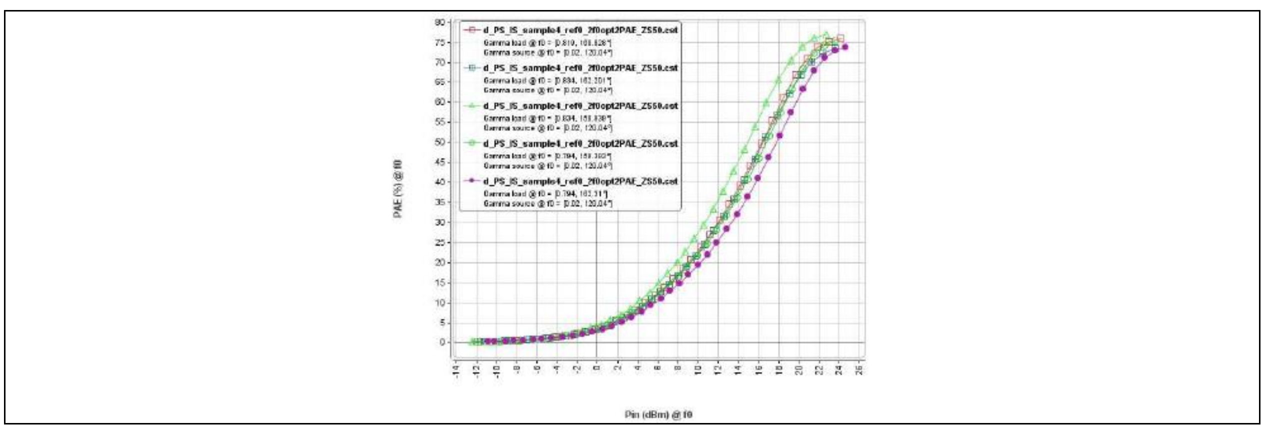

Figure 41 : Measurements @ 1.57 GHz with Vds0=45V Ids0=400mA (25mA/mm), Power Bar reference plane, power bar n°4. PAE(%) vs Pin(dBm)

Load pull measurements demonstrate that power bar 8x8x250µm could reach more than 67% PAE (sample 2) in the SMA connectors and more than 77% (sample 2) in the power bar plan. The maximum PAE was obtained with a superior 60W output power. The two samples presented in this manuscript (sample 4 and sample 2) have equivalent performance (Pout, PAE, Power Gain, ...). The optimum impedances area is the same.

2.1.3.4 Power Bar modeling activity. Run-1

The objectives have consisted to validate the nonlinear electro-thermal model of the power bar 8x8x250µm based on UMS GH50_10 technology. The power bar is based on the assembly of 8 transistors of GH50_10 Technology. Each transistor is made of 8 fingers of 250µm width. The electrical part of the transistor model has been performed by AMCAD Engineering, the thermal part by XLIM. This report takes into account of the results obtained and mentioned in the AMCAD and XLIM reports. Loadpull measurements performed by AMCAD for the power bar have been used for extraction as well as TAS simulations. The test set is presented in figure below. Two types of measurements have been considered: deem bedded or in the SMA connector planes. The deem bedding circuits have been either measured by AMCAD or simulated by TAS.

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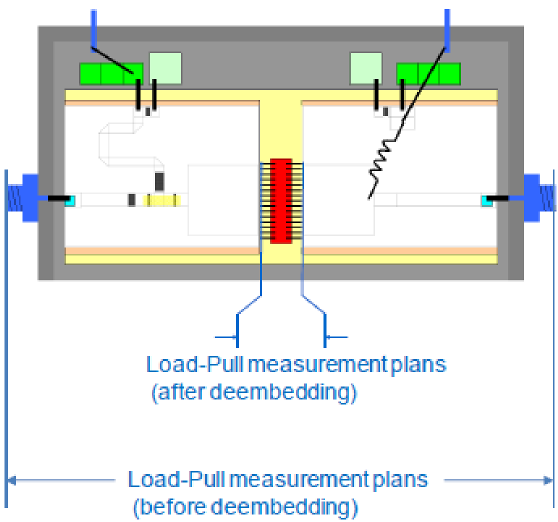
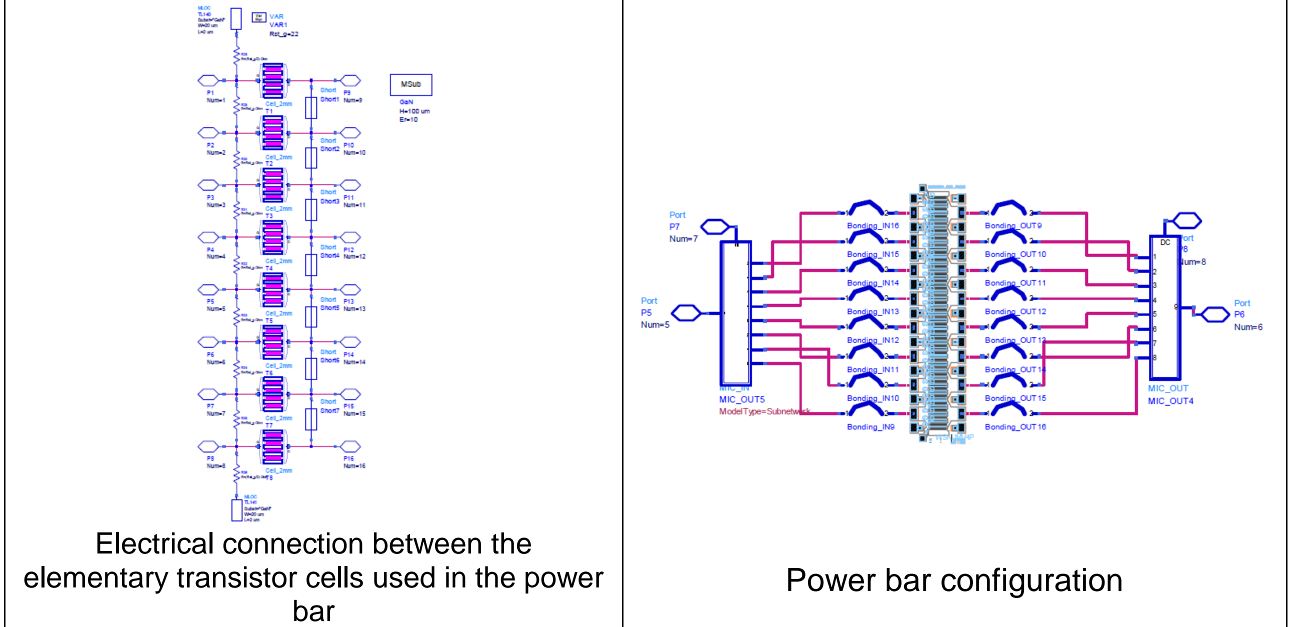


Figure 42 : Measurement test set off the power bar

The 2mm elementary transistor cells are connected at the drain with a short circuit and connected through a resistor at the gate as shown in figure below. According to the thermal study performed by XLIM, coupling circuit are necessary between the elementary transistor cells. For measuring this power bar, an input circuit and an output circuit have been added. The power bar is connected through wire bondings to input and output circuit as shown in figure below. Wire bondings are represented by their S parameters. Input circuit and output circuit are represented either by what a simulated circuit or S parameters of these circuits.



Electrical connection between the elementary transistor cells used in the power bar	Power bar configuration

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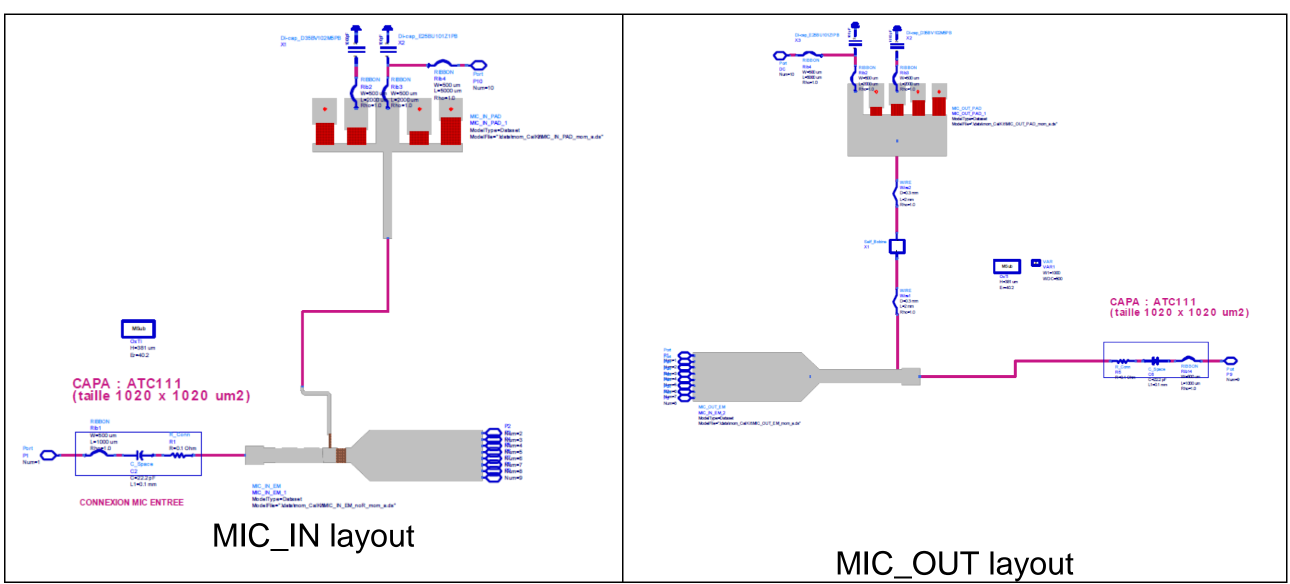

Figure 43 : Electro thermal Model of the Power bar

For measurements and simulations comparison, 3 samples have been considered. They are called sample 2, 4 and 5 to keep the same names as those given by AMCAD during measurements.
A first simulation has been performed in the SMA connector planes. This simulation reveals results which are not sensitive to variation of power bar parameters.
Then, simulation have been performed in the power bar reference plan: deem bedded results before wire bondings for the input and after wire bondings in output have been considered.
Several cases have been considered to sweep loads in term of power optimization or PAE optimization. The results are presented below for sample n°4. The results presented are the output power versus the input power, the PAE versus the input power the DC drain current, the power gain, and the Gamma in (input reflection coefficient). The time domain waveform of current and drain voltage is also presented.

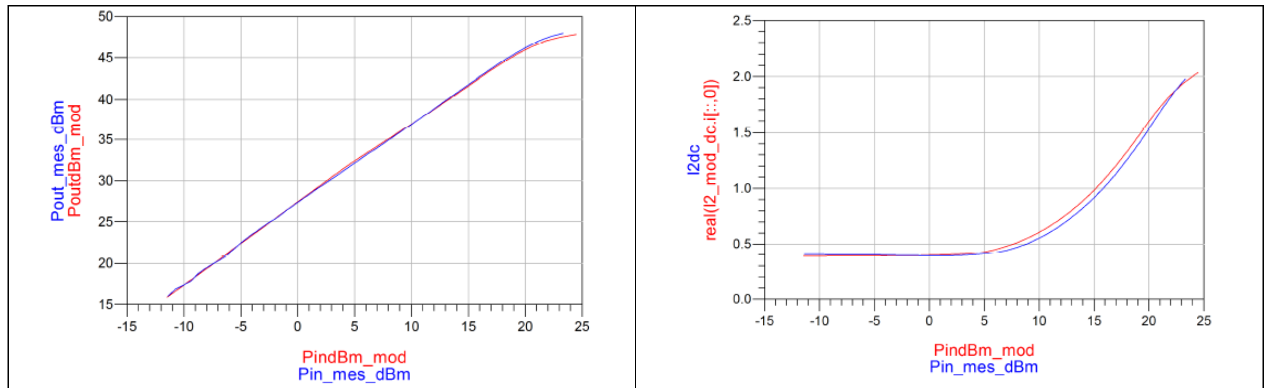

Figure 44 : Pout vs Pin and DC drain current versus vs Pin. Comparison between simulation and measurements for power bar sample4

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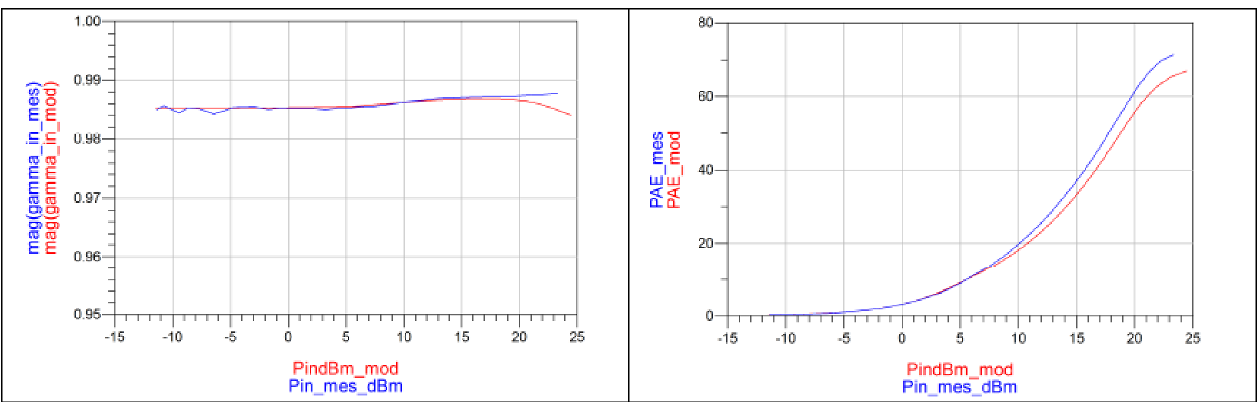

Figure 45 : Input reflection coefficient versus Pin and PAE versus Pin. Comparison between simulation and measurements for power bar sample4

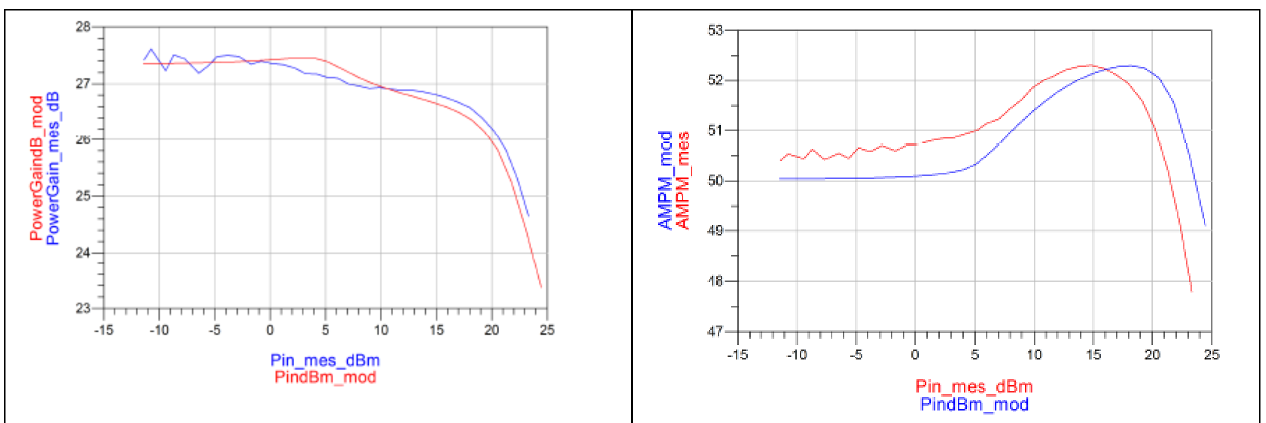

Figure 46 : Power Gain vs Pin and AMPM vs Pin. Comparison between simulation and measurements for power bar sample4

Comparing measurement to simulation obtained from the nonlinear electro-thermal model lead to the following remarks:

- It is crucial to perform the comparison in the plane where changes in the model parameters provide reasonable changes in the observed performances. Clearly, connector planes are not adequate for this.
- Wire bondings must be accurately modeled mainly from the point of view of the losses as they largely impact the input reflection coefficient of the power bar which is close to 1. When the losses of the input are poorly modeled, they must be compensated in the simulation to reach consistent results.
- On key point which still remains unclear is the behavior of the drain current as the input power increases the modeled one is always larger than the measured one. This could be due to traps that are activated when the device reaches pinch-off and reduce the current, but this phenomenon does not clearly appears in the unit cell. Works still have to be performed on this particular point.

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2.1.4 Detailed Design. Run-1

Starting from baseline design performed in WP3100 and presented in chapter 2.1.1, design has been finalized with NL electro-thermal model of the power bar provided by AMCAD and XLIM.
Simulations results are presented in this report:

- S-Parameters simulations
- Non-linear simulations with CW signal
- Stability analysis (STAN)
- HPA analysis with multicarrier signal

Design of the HPA has been undertaken to reach the best possible performances with priority on PAE.First of all, optimal output load impedances at fundamental, second and third harmonic frequency have been searched and identified
GH50 technology enables designs up to 53.3V (AMR) of drain voltage. In the following study, spatial derating ratio of 75% has been applied regarding AMR drain voltage, leading to a maximum biasing drain voltage VD0 = 40V. This value has been confirmed by UMS. According to the baseline design , load-pull measurements and simulations have been compared at the following transistor quiescent point:

Frequency	Vdso	Idso	Simulation type
1.57 GHz	40 V	25 mA/mm	CW

Optimum 8x250µm transistor output loads have been determined at both fundamental (H1) and second harmonic (H2) frequency using AMCAD 8x250µm transistor load-pull measurements data of baseline design. In addition, load-pull simulations with both UMS and AMCAD transistor models have been performed to confirm these data.
Crossing load-pull measurements and simulation results at transistor level have allowed us to define an optimum load impedance area at both H1 and H2.

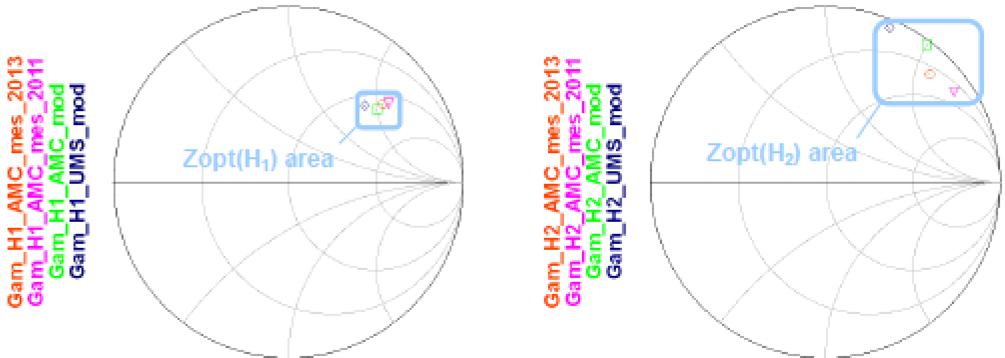

Figure 47 : Optimal load impedances found at fundamental (left) and 2nd harmonic (right) frequencies based on 8x250µm transistor load-pull measurements and simulations.

As a result, Zopt(H1) & Zopt(H2) area have been taken as load impedance goals to design the HPA. Load-pull measurements have pointed out that PAE performances are not sensitive to the third harmonic frequency over a wide load impedance area

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(±2%). This is the reason why the Zopt(H3) area have been optimized to be kept in this sweet spot area during the HPA design.
In order to optimize and predict accurately the HPA performances, package RF insert, capacitors and inductors have been carefully simulated and/or measured to secure the design result.
To simulate input and output package RF ports, simulations have been performed using insert model based on HFSS 3D electromagnetic simulations.

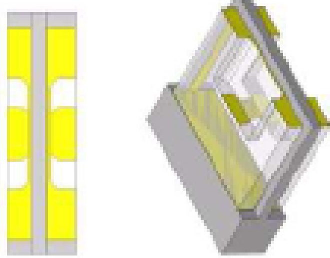

Figure 48 : Overview of the RF insert used with the CuD package

In order to optimize the simulation results, homemade discrete capacitors model have been used whereas S-parameter files (coming from measurements data) have been used to simulate discrete self inductors used for DC biasing. Due to both input and output matching networks size constraints and the need of high distributed capacitance effect to synthesize appropriate input and output load impedances, high dielectric constant material has been used : Er =40; T=381µm; TanD=0.0003
Input and output combiners have been fully optimized by means of EM simulation up to 10GHz. Engrave resistance sheet has been chosen as low as possible (6W/□) to enable the design of resistors in series with the gate of each transistor. In this way, both even and odd mode stability issues have been managed at the same time.

The following figures shows the small signal behavior of the HPA in a wide frequency range

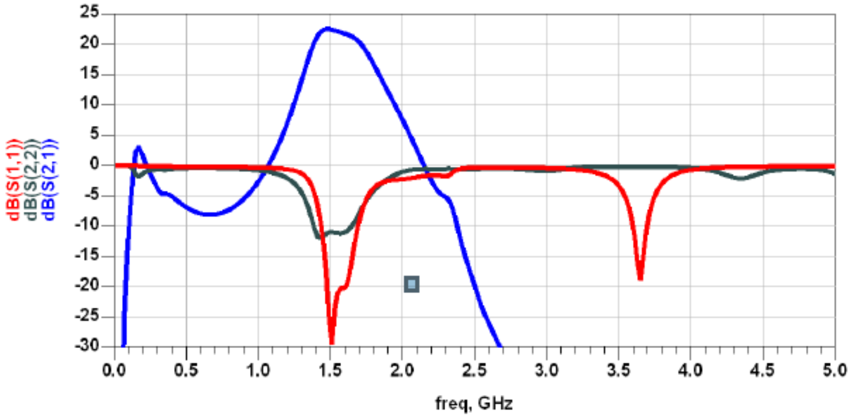

Figure 49 : S-parameters wide frequency band analysis

S21 parameter drops below 0dB for frequency higher than 2.2GHz. HPA design

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have been managed to break the very high gain of the power bar at frequency below 1GHz. In that way, low frequency and Fo/2 oscillation issues will be prevented.

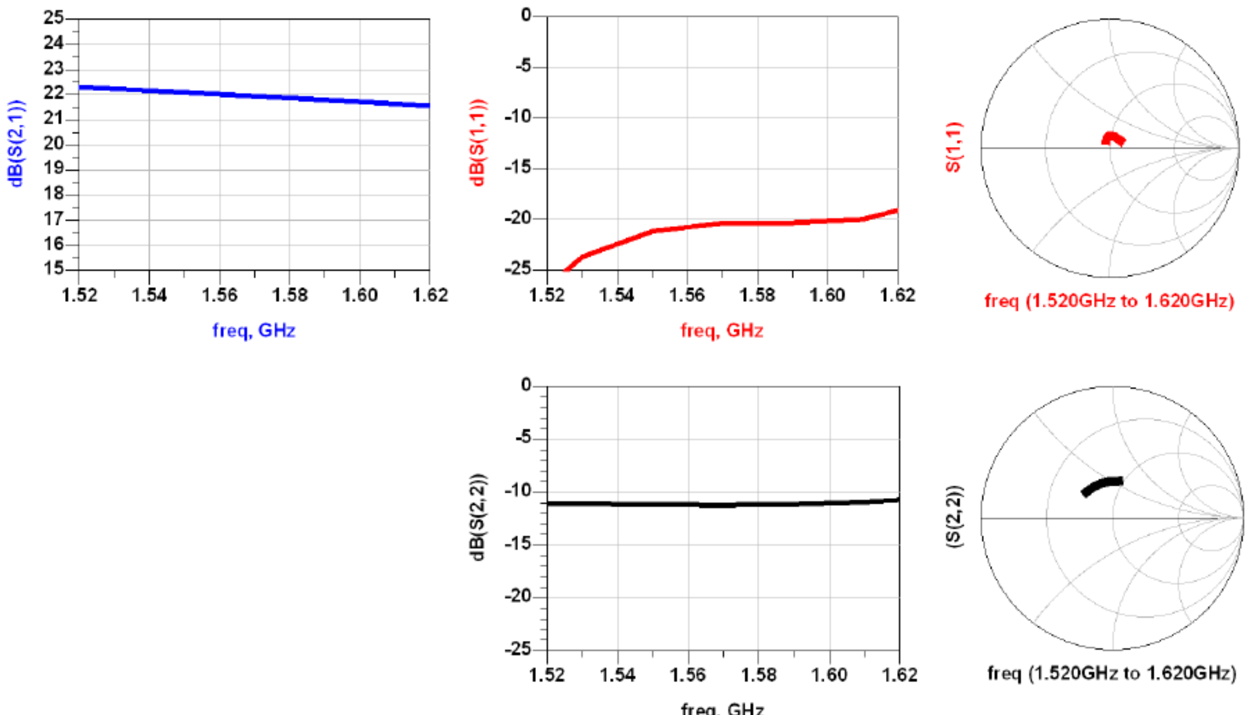

Figure 50 : S-parameters in-band frequency analysis

We can see that the HPA exhibits a S21 of 22dB at center frequency with a slight negative slop over the frequency bandwidth of interest. In addition, we can focus on the S11 that have been optimized to enable an in-band input return loss better than -20dB.

The necessary and sufficient conditions for unconditional stability are that the K stability factor is greater than unity and the B stability measure is positive. K factor and B stability measure are given below. According to the unconditional stability definition, no stability issues have been highlighted at small signal level.

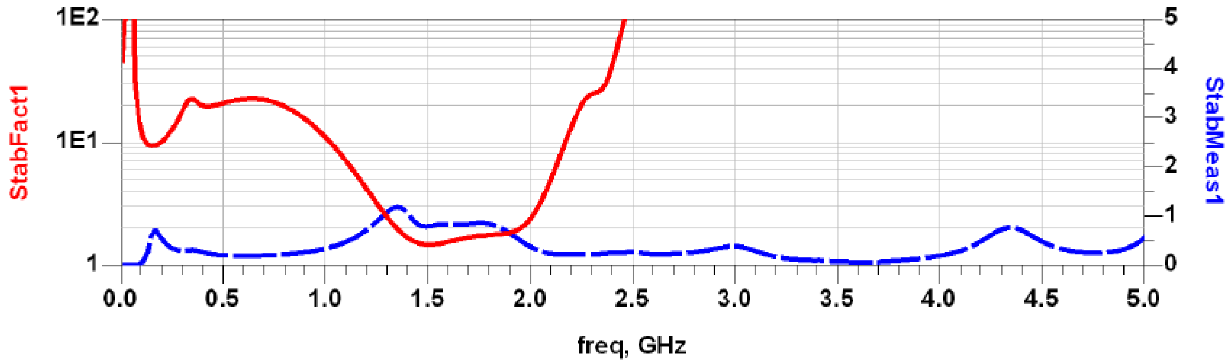

Figure 51 : K stability factor & B stability measurements. Wide frequency band analysis.

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To point out the consistency of the HPA optimization, synthesized output load impedances at H1 and H2 are shown below.

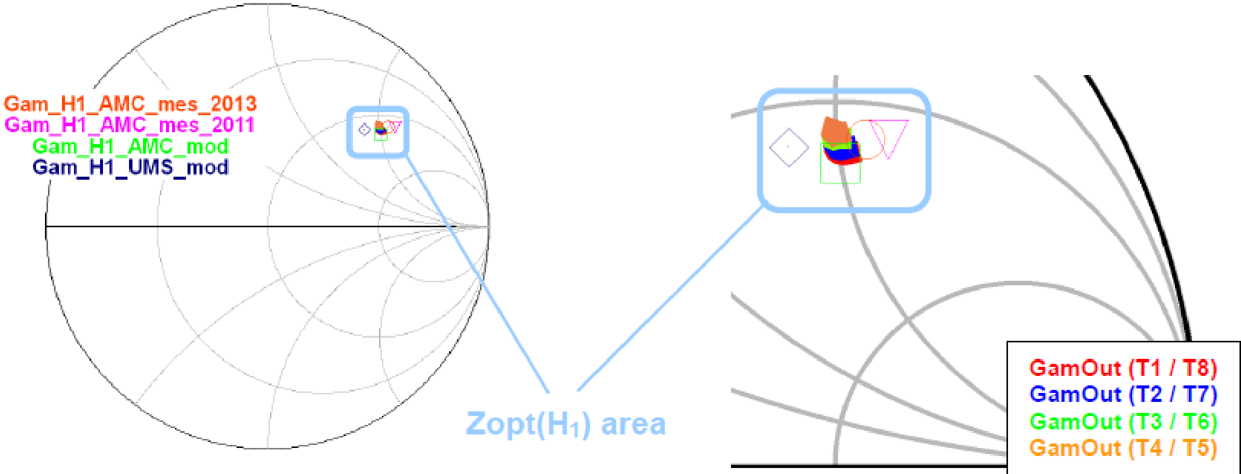

Figure 52 : Synthesized output impedances at fundamental frequency (H1) from 1.52GHz to 1.62GHz

Previous figure shows the load impedances synthesized at the output of each transistor of the 8x8x250µm power-bar. Due to the symmetry of the output combiner design, impedances of the transistor are superimposed 2 by 2. Zload(H1) between elementary transistor are very well balanced and perfectly match the targeted load impedance area.
Regarding 2nd harmonic load impedance behavior we can see that, again, even at H2 frequency all the transistors exhibits a very good load impedances balance. The targeted impedance area is also matched.

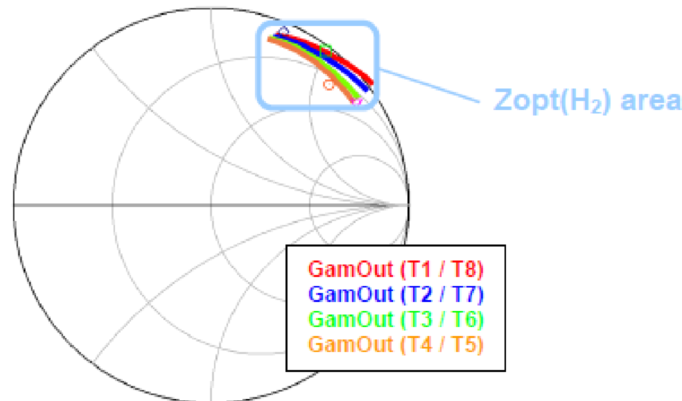

Figure 53 : Synthesized output impedances at 2nd harmonic frequency (H2) from 3.04GHz to 3.24GHz

Note that the design enable H2 load impedance tuning quasi-independently of the load impedance at the fundamental frequency by connecting metallization pads.

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On top of that, output losses are given versus frequency on Figure 54, with input power in parameter. This confirm that low losses are simulated which should ensure PAE performances.

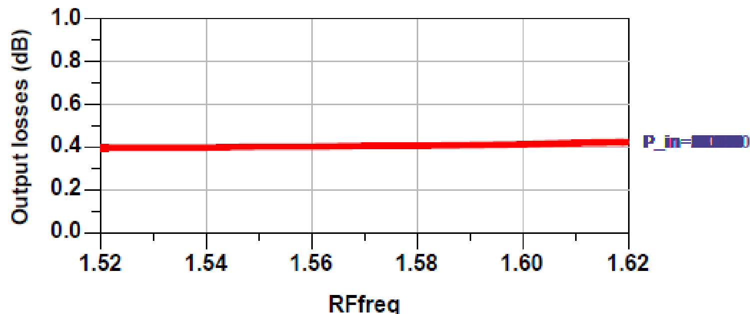

Figure 54 : Output combiner losses (dB) versus RFfreq and input power(dBm)

The main RF performances obtained, output power, PAE and power gain are presented below versus input power and versus frequency.

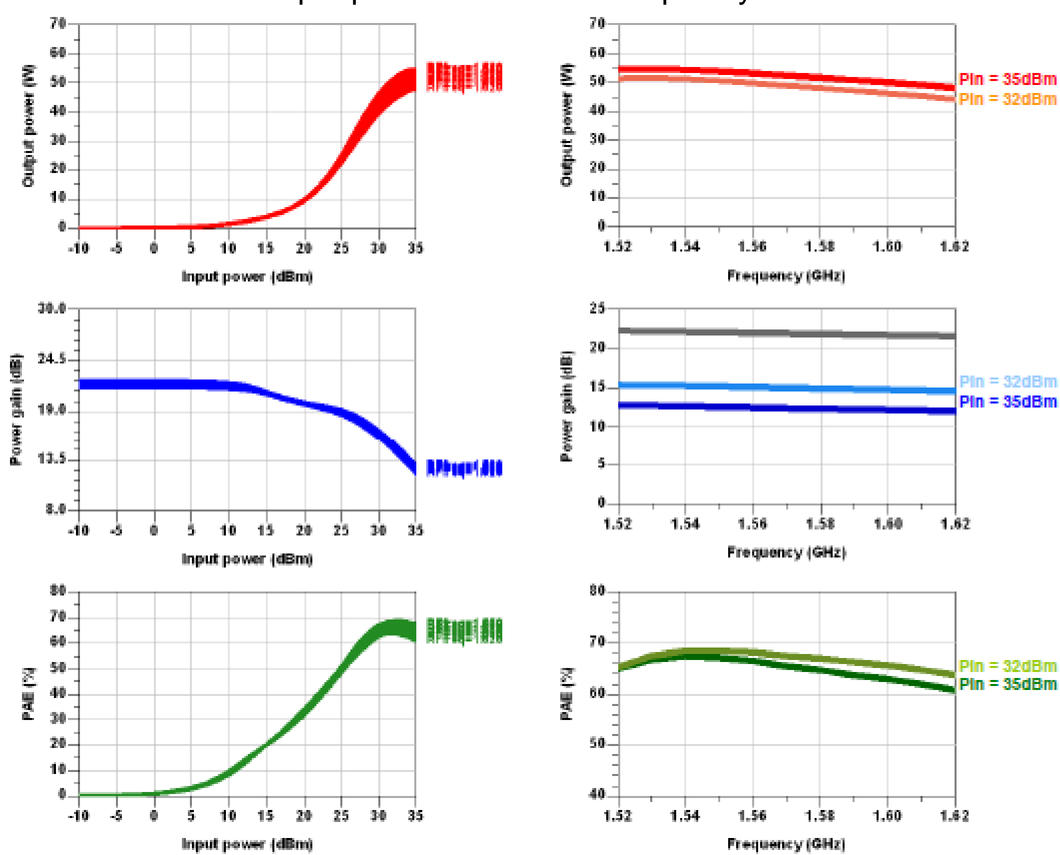

Figure 55 : HPA RF performances. Pout(W), PAE(%), Gain(dB) versus input power (dBm) and Frequency(GHz).

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The frequency bandwidth reaches 100MHz for a center frequency of 1.57GHz. The maximum overall power added efficiency varies from 65 to 68% at Pin = 32dBm and is associated to an output power of 45W to 52W. Figure 56 below, shows that between 32dBm and 35dBm of input power, the mean output power density is around 3.5W/mm.

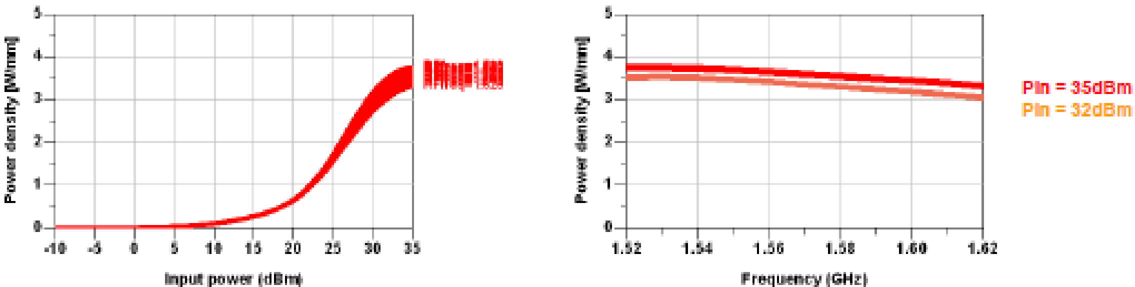

Figure 56 : Drain current and power consumption(W) vs. input power(dBm) – from 1.52 to 1.65GHz

DC drain and gate currents as well as DC power consumption have been drawn on figure below.

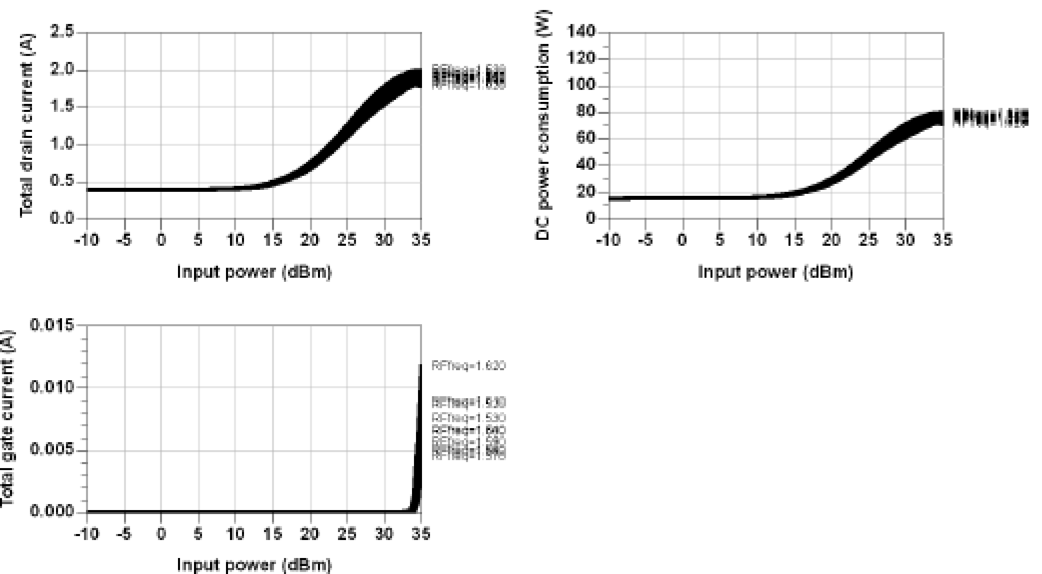

Figure 57 : Drain current and power consumption(W) vs. input power(dBm) – from 1.52 to 1.65GHz

Thanks to the electro-thermal capability of the transistor model, the main RF performances; output power, PAE and power gain; of HPA has been checked versus a temperature range from -10°C to 85°C. Main HPA performances are shown for an input power (@32dBm) corresponding to the maximum of PAE (Pin = 32dBm)

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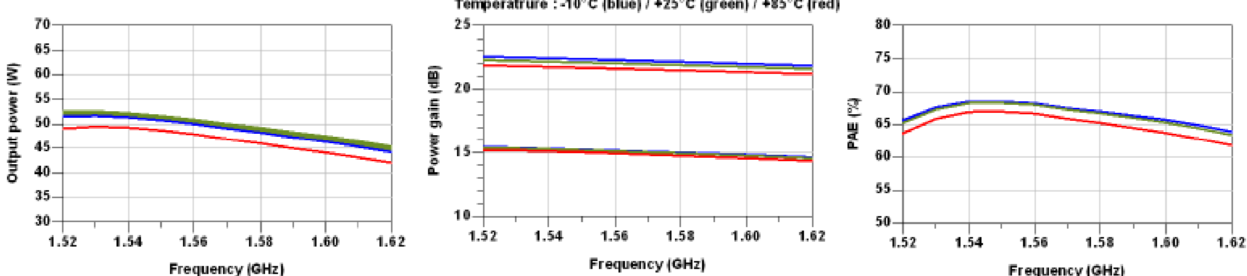

Figure 58 : HPA performances : Pout(W), PAE(%), Gain(dB) versus temperature [-10°C; 25°C, 85°C] @Pin(max PAE).

Performances are not very sensitive to the temperature, and RF performances slightly decrease by - 0.2dB on Pout and -2pts on PAE at high temperature. This phenomenon is mainly due to the power gain level drop as a function of the temperature.

HPA non-linear stability analysis has been performed using STAN software. Current probe was placed on transistor gate. The STAN aalysis setup is given below:

- Temperature applied on transistor model: -10°C (wo rst case)
- Frequency pump (Fp): 1.57 GHz, 1.54 GHz, 1.6 GHz
- Frequency Band Analysis (FBA) : [0.05-2GHz]
- Nb of points within FBA: 300 up (arbitrary 15 to 20MHz step)
- Input power sweep (for each Fp) : [10 to 32]dBm / step 1dB
- Max. phase error tolerance : 10-1

According to results monitored during stability analysis, NO stability issues have been highlighted. Nevertheless, we have to point out that these results have to be taken with care because the transistor model is only validated for a drain voltage of 40V. Thus, all others drain voltage simulation results are extrapolated.

Finally, a Volti analysis has been done at HPA level to check the feasibility of the PAE, output power, NPR trade-off. Quiescent point used for multi-carrier simulation are: Vds=40V and Ids=25mA/mm. On the following figure, PAE, NPR and gain compression are drawn versus output power.

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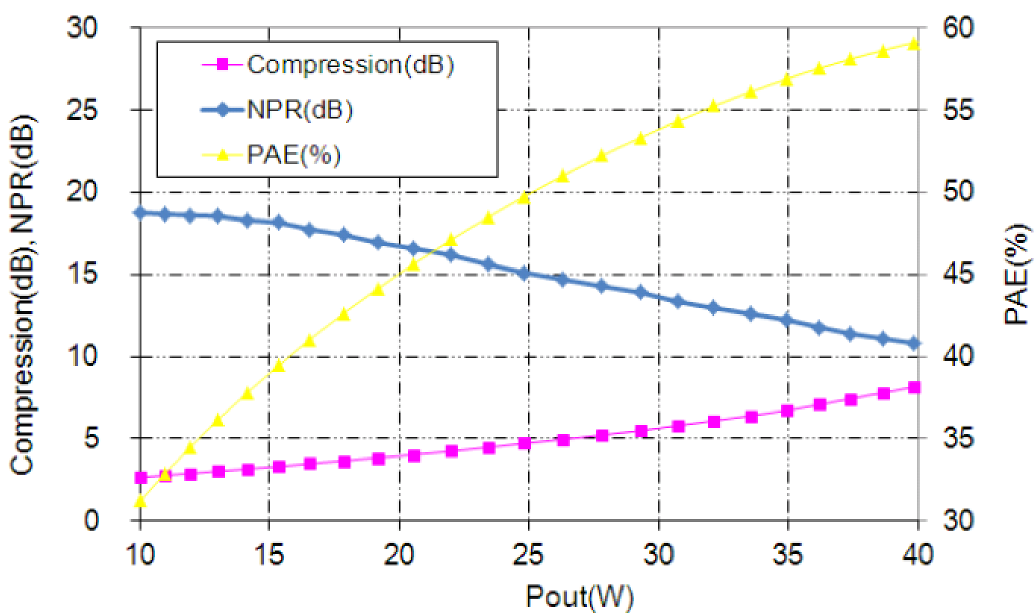

Figure 59 : HPA performances in multi-carrier mode : NPR(dB), compression(dB), PAE(%) versus Pin. Temp=25°C, Vds=40V and Ids=25mA/mm

RF SECTION		Gain	Cumul Gain	NF	Cumul NF	Signal Level	Signal level	NPR	Pdc	Pdiss	PAE	EPC	Gain Comp
N°	Elements	dB	dB	dB	dB	dBm	W	dB	W	W	%	N°	dB
	INPUT					27,00	5,01E-01						
1	Fixed ATT	0,00	0,00	0,00	0,00	27,00	0,5012	387,60	0,00	0,00	0,00		0,00
2	HPA_40V_VG_1_85V	16,96	16,96	10,00	10,00	43,96	24,8684	15,18	46,44	22,07	52,47	3	4,71
	Total RF Section		16,96		10,00	43,96	24,87	15,18	46,44	22,07	52,47		4,71

Table 11 : HPA performances in multicarrier mode @NPR=15dB. Temp=25°C. Vds=40V, Ids=25mA/mm

RF SECTION		Gain	Cumul Gain	NF	Cumul NF	Signal Level	Signal level	NPR	Pdc	Pdiss	PAE	EPC	Gain Comp
N°	Elements	dB	dB	dB	dB	dBm	W	dB	W	W	%	N°	dB
	INPUT					27,50	5,62E-01						
1	Fixed ATT	0,00	0,00	0,00	0,00	27,50	0,5623	398,93	0,00	0,00	0,00		0,00
2	HPA_45V_VG_1_85V	17,45	17,45	10,00	10,00	44,95	31,2862	15,05	58,43	27,71	52,58	3	4,57
	Total RF Section		17,45		10,00	44,95	31,29	15,05	58,43	27,71	52,58		4,57

Table 12 : HPA performances in multicarrier mode @NPR=15dB. Temp=25°C. Vds=45V, Ids=30mA/mm

Main performances (Pout/PAE/NPR) in multicarrier mode are compliant with specifications by using the quiescent point Vds=45V and Ids=30mA/mm

Following tables summarize the HPA performances reached for the center frequency 1.57GHz in both CW and multi-carriers mode.

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CW mode : PAE peak performance for an input power of 32dBm. Vds=40V and Ids=25mA/mm.	
Parameters	**Typ.**
Output Power	50W
PAE	67%
Gain compression	7dBcomp (15dB)
Dissipated power	25W

Table 13 : Summary of simulated CW performances at HPA level

In CW mode, the simulated HPA performances match the RF specifications 50W output power and more than 65% of peak PAE in the 1.52GHz-1.62GHz bandwidth at 32dBm of input power. These performances are associated to a power gain of 15dB.

Multi-carrier mode : VOLTI analysis Vds=45V and Ids=30mA/mm.	
Parameters	**Typ.**
Output Power	**31.3W**
PAE	**52,5%**
Gain compression	**4,5dB**
NPR	**15dB**

Table 14 : Summary of simulated multi-carriers performances at HPA level

In multi-carrier mode with NPR=15dB, the simulated HPA performances match the RF specification of 30W output power and more than 52% of PAE in the 1.52GHz-1.62GHz bandwidth. These performances are associated to a power gain of 17,5dB.

2.1.5 HPA-1 Module Manufacturing and Tests. Run-1

This paragraph establishes the report of tests performed on 3 L-band GaN HPA Modules.
3x L-band GaN HPA modules have been manufactured and tested: HPA#2 HPA#3 HPA#5. In the frame of this study, tuning of the HPA modules has been performed at Temp=25°C with CW signal in order to achieve maximum of PAE. Then [S] parameter measurements and power measurements with multi-carrier signal has been conducted.
The results are presented with the following outline

- [S] parameters measurements versus Temp=[-20°C , 25°C , 90°C] for HPA#2 module
- [S] parameter measurements versus Vd=[20V/25V/30V/40V/45V]. Temp=25°C for HPA#2 module.

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- [S] parameters measurements versus Temp=[-20°C , 25°C , 90°C] for three HPA modules
- Power measurements (CW signal) versus Pin. Temp=[-20°C , 25°C , 90°C]. Vds=40V and Vds=45V, RF=[1,5425GHz / 1,5675GHz / 1,5925GHz] for three HPA modules
- Power measurements versus Pin. Temp=[25°C , 90°C]. Vds=45V, RF=1,5675GHz, Ids=[100mA / 200mA / 400mA / 800mA] for HPA#5 module
- Power measurements (multi-carrier signal) versus Pin. Temp=[-20°C , 25°C , 90°C]. Vds=45V. Ids=[100mA / 200mA / 400mA / 800mA] for HPA#5 module
- RF step stress measurements for three HPA module

2.1.5.1 [S] Parameter measurements. Run-1

Hereafter, on figure below the HPA-1 module (#2) S-parameters are given over a DC to 10GHz bandwidth with drain voltage of 45V and Ids=400mA (25mA/mm) fixed at Temp=25°C . Measurements are performed versus Temp=[-20°C , 25°C , 90°C]

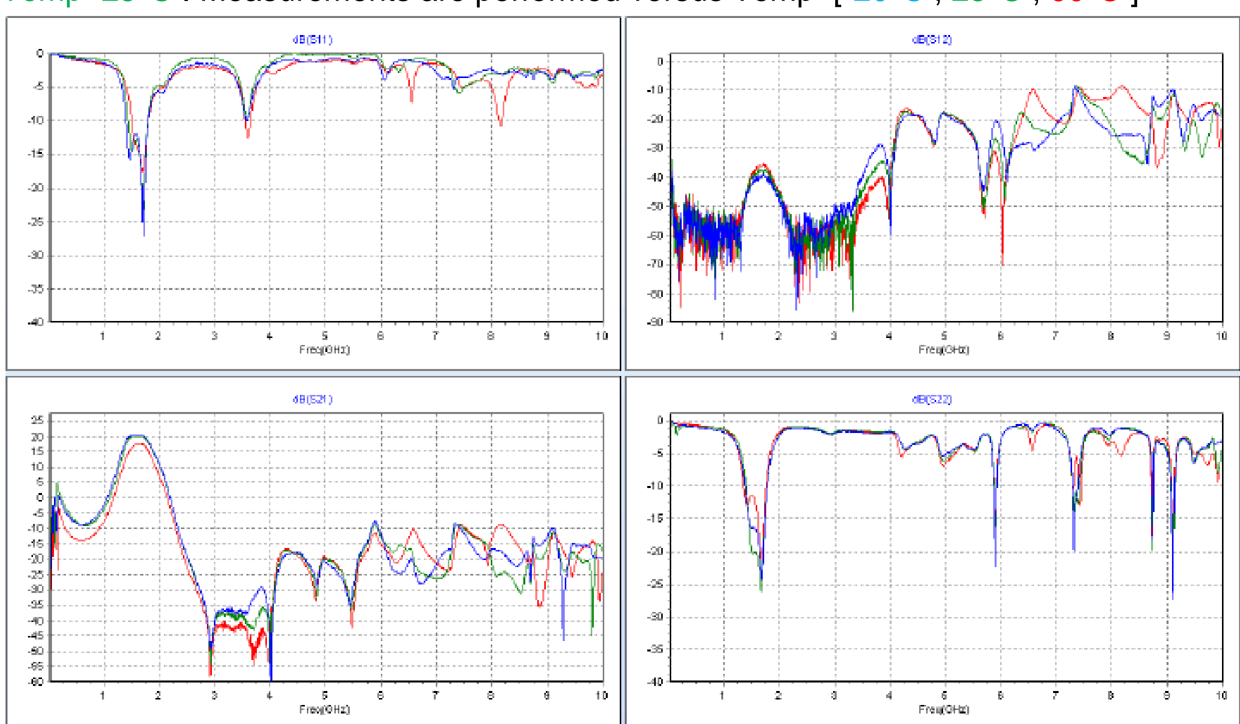

Figure 60 : HPA-1 module (#2). [S] parameters measurements. RF=[DC-10GHz], Vd=45V, Fixed drain current Ids=400mA @25°C , Temp=[-20°C , 25°C , 90°C]

On following figures, we focus on the HPA-1 module (#2) in-band frequency behavior. Figure shows that S11 and S22 parameters varies not in the same way:

- Input return loss is optimum at hot temperature
- Output return loss is optimum at room temperature.

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S21 variation is about 3dB between -20°C to 90°C at 1 .55GHz. At constant gate voltage current, the gain variation versus temperature is 0,25dB/°C.

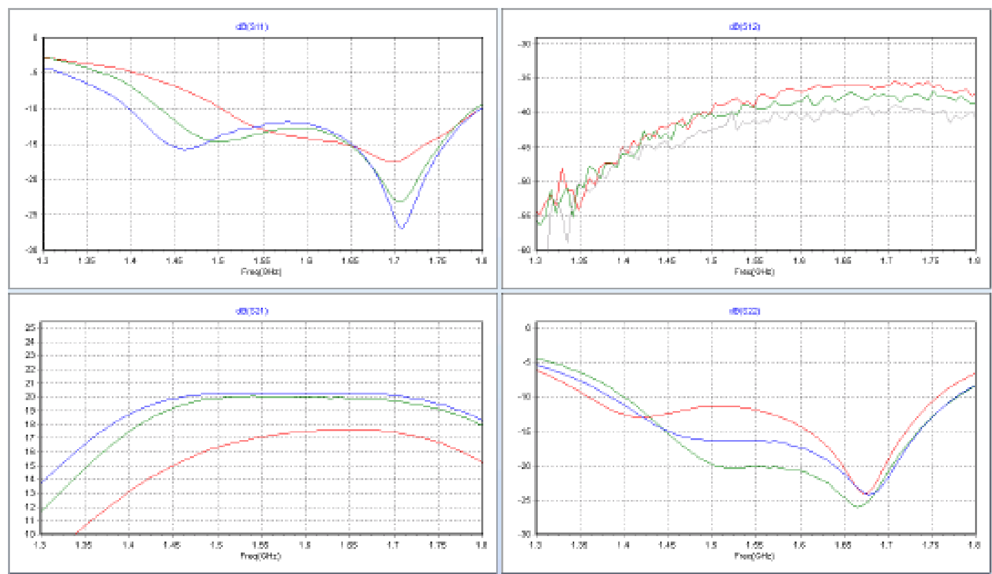

Figure 61 : HPA-1 module (#2). [S] parameters measurements. RF=[1.3-1.8GHz], Vd=45V, Fixed drain current Ids=400mA @25°C , Temp=[-20°C , 25°C , 90°C]

On following figures, we focus on the HPA#2 module in-band frequency behavior versus drain voltage variation. Figures show that S22 parameters varies versus drain voltage value and is optimum at Vds=40V. S21 variation is about 4dB between 20V to 45V at 1.55GHz. At constant gate voltage current, the gain variation versus drain voltage value is 0,16dB/V.

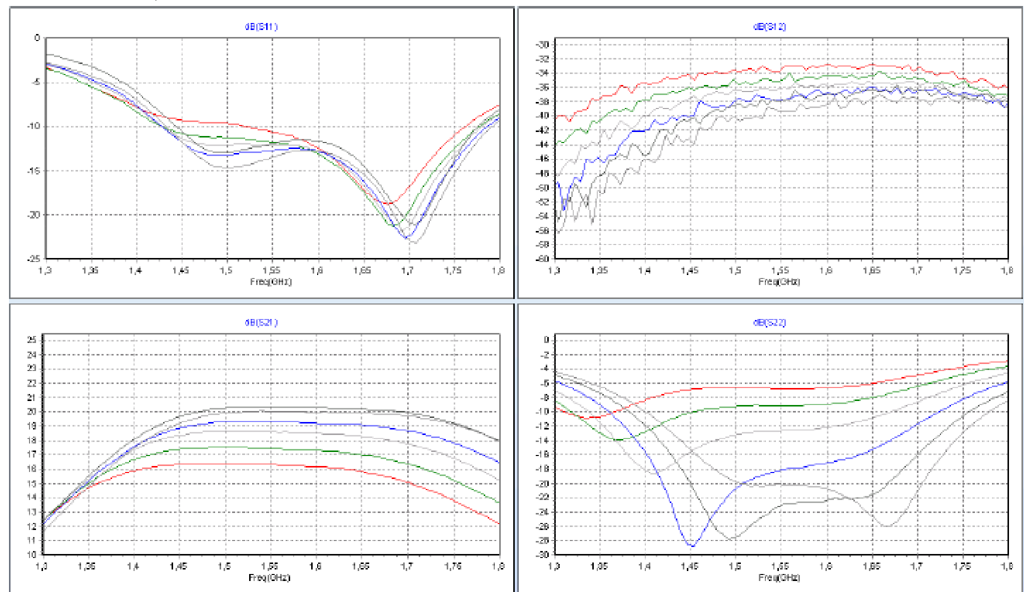

Figure 62 : HPA-1 module (#2). [S] parameters measurements. RF=[1.3-1.8GHz], Vd=[20V/25V/30V/40V/45V]. Fixed drain current Ids=400mA @25°C . Temp=25°C

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Hereafter, for three HPA modules, the S-parameters are given over a DC to 10GHz bandwidth with drain voltage of 45V and Ids=400mA (25mA/mm) fixed at Temp=25°C. Measurements are performed versus Temp=[-20°C , 25°C , 90°C]

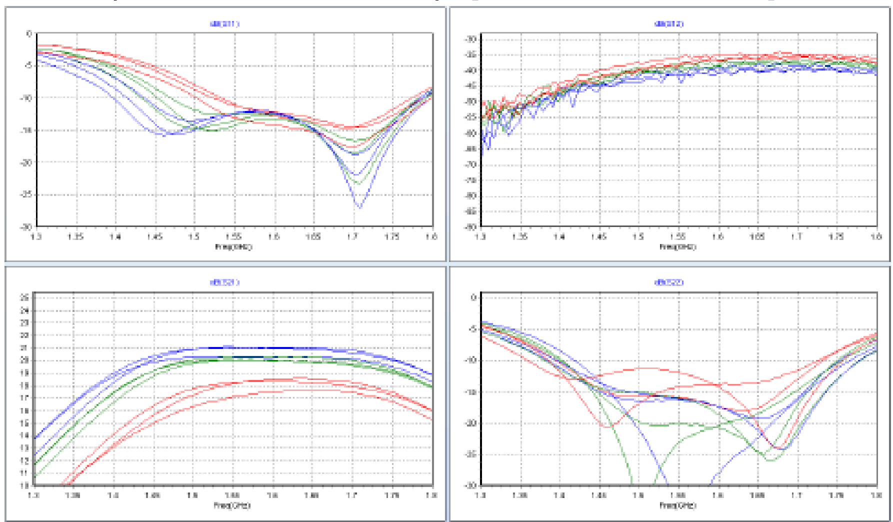

Figure 63 : HPA-1 modules (#2#3#5). [S] parameters measurements. RF=[1.3-1.8GHz], Vd=45V, Drain current Ids=400mA @25°C . Temp=[-20°C , 25°C , 90°C].

Regarding S21 parameter, at 1,55GHz, a maximum dispersion of 1dB is observed between the three HPA modules. Regarding S11 parameter, at 1,55GHz, a maximum dispersion of 2dB is observed between the three HPA modules. Regarding S22 parameter, dispersion is higher compared to the previous parameters. Indeed, depending of the HPA modules, the settings applied on the output combiner to obtain maximum of PAE have an impact of the output return loss behavior.

2.1.5.2 CW mode power measurements. Run-1

The main RF performances obtained, output power, PAE, power gain and phase are presented below versus input power and three frequency points [1,5425GHz, 1,5675GHz, 1,5925GHz]. Measurements have been performed versus Temp=[-20°C , 25°C , 90°C]. For each frequency and each temperature, drain current has been tuned in small signal: Ids=400mA with Vds=40V.

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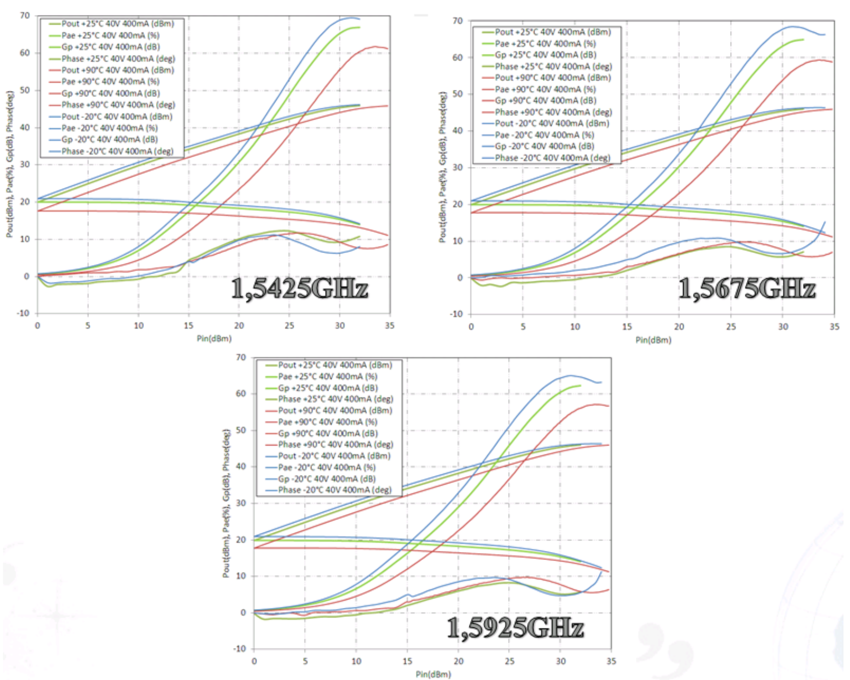

Figure 64 : HPA-1 module (#2). Power measurements with CW signal. Temp=[-20°C, 25°C, 90°C], Vd=40V, Id=400mA. RF=[1,5425GHz/1,5675GHz/1,5925GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

In figure below, the results (Pout, Gain, PAE) are presented versus frequency and temperature. Pin is fixed to obtain maximum of PAE.

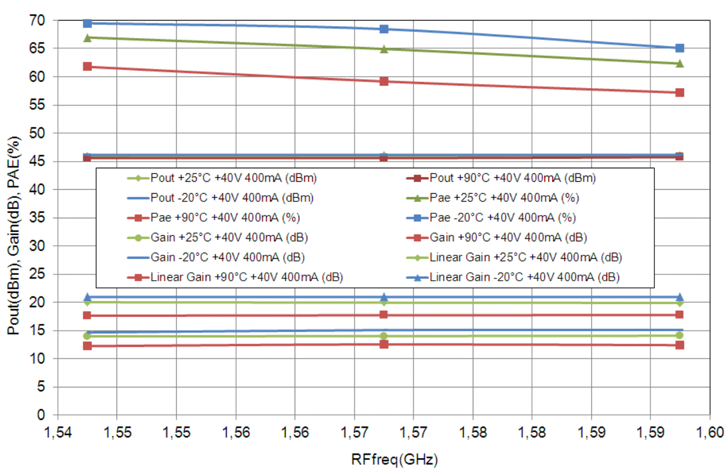

Figure 65 : HPA-1 module (#2). Power measurements with CW signal. Temp=[-20°C, 25°C, 90°C], Vd=40V, Id=400mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

At Vds=40V and room temperature, the maximum overall power added efficiency varies from 62 to 67% and is associated to an output power of 39,4W to 40,4W.

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The main RF performances obtained, output power, PAE, power gain and phase are presented below versus input power and three frequency points [1,5425GHz, 1,5675GHz, 1,5925GHz]. Measurements have been performed versus Temp=[-20°C, 25°C, 90°C]. For each frequency and each temperature, drain current has been tuned in small signal: Ids=400mA with Vds=45V.

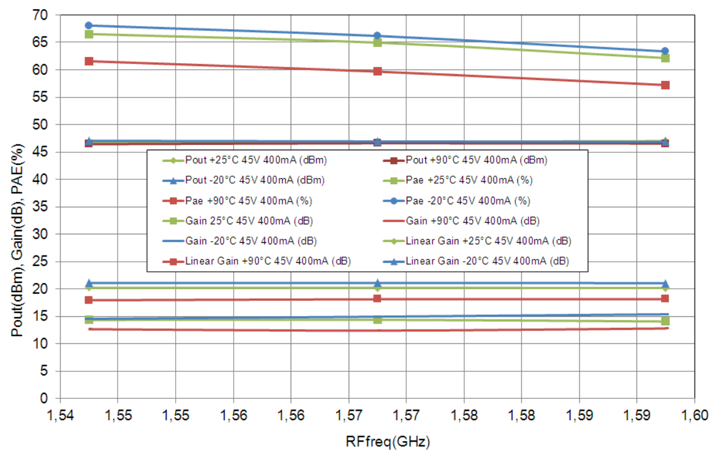

Figure 66 : HPA-1 module (#2). Power measurements with CW signal. Temp=[-20°C, 25°C, 90°C], Vd=45V, Id=400mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

At Vds=45V and room temperature, the maximum overall power added efficiency varies from 62 to 66,5% and is associated to an output power of 48,2W to 50W.
Synthesis of the RF performances measured with CW signal are provided in the following table

Temp (°C)	Biasing Point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
90	Vd=40V, Id=400mA	1,54	17,63	45,61	36,39	2,27	61,76	12,24	5,39
		1,57	17,71	45,57	36,06	2,25	59,17	12,55	5,16
		1,59	17,75	45,75	37,58	2,35	57,19	12,41	5,34
25	Vd=40V, Id=400mA	1,54	20,03	45,95	39,36	2,46	66,97	13,97	6,06
		1,57	19,95	46,01	39,90	2,49	64,93	14,02	5,93
		1,59	19,90	46,06	40,36	2,52	62,33	14,08	5,82
-20	Vd=40V, Id=400mA	1,54	20,96	46,14	41,11	2,57	69,49	14,66	6,30
		1,57	20,97	46,15	41,21	2,58	68,45	15,08	5,89
		1,59	20,94	46,14	41,11	2,57	65,10	15,12	5,82

Temp (°C)	Biasing Point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
90	Vd=45V, Id=400mA	1,54	17,94	46,43	43,95	2,75	61,57	12,65	5,29
		1,57	18,12	46,60	45,71	2,86	59,67	12,40	5,72
		1,59	18,12	46,55	45,19	2,82	57,21	12,79	5,33
25	Vd=45V, Id=400mA	1,54	20,23	46,83	48,19	3,01	66,53	14,34	5,89
		1,57	20,22	46,87	48,64	3,04	64,96	14,38	5,84
		1,59	20,17	46,99	50,00	3,13	62,15	14,06	6,11
-20	Vd=45V, Id=400mA	1,54	21,08	47,04	50,58	3,16	68,09	14,54	6,54
		1,57	21,10	46,94	49,43	3,09	66,18	14,94	6,16
		1,59	21,07	46,85	48,42	3,03	63,36	15,38	5,69

Table 15 : HPA-1 module (#2). Synthesis of power measurements with CW signal. Temp=[-20°C, 25°C, 90°C], Vd=40V & Vd=45V, Id=400mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

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HPA-1 modules (#3 and #5) have been tested with the same approach. Synthesis of the measurements results are presented in the table below.

Temp (°C)	Biasing Point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
90	Vd=40V, Id=400mA	1,54	17,54	45,59	36,22	2,26	58,62	11,68	5,86
		1,57	17,76	45,94	39,26	2,45	63,70	11,99	5,77
		1,59	17,86	46,00	39,81	2,49	62,22	12,09	5,77
25	Vd=40V, Id=400mA	1,54	20,04	46,51	44,77	2,80	58,41	12,50	7,54
		1,57	20,07	46,71	46,88	2,93	66,02	13,65	6,42
		1,59	20,05	46,81	47,97	3,00	67,64	12,81	7,24
25	Vd=40V, Id=400mA	1,54	20,94	46,36	43,25	2,70	55,87	13,32	7,62
		1,57	20,83	46,66	46,34	2,90	63,32	13,62	7,21
		1,59	20,93	46,71	46,88	2,93	67,16	14,70	6,23

Temp (°C)	Biasing Point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
90	Vd=45V, Id=400mA	1,54	18,00	46,20	41,69	2,61	54,23	11,75	6,25
		1,57	18,23	46,75	47,32	2,96	62,35	12,31	5,92
		1,59	18,34	46,88	48,75	3,05	62,45	12,46	5,88
25	Vd=45V, Id=400mA	1,54	20,28	46,97	49,77	3,11	53,33	12,44	7,84
		1,57	20,31	47,39	54,83	3,43	61,94	13,38	6,93
		1,59	20,30	47,53	56,62	3,54	65,66	14,06	6,24
25	Vd=45V, Id=400mA	1,54	21,07	46,78	47,64	2,98	51,30	13,24	7,83
		1,57	21,12	47,21	52,60	3,29	59,64	14,16	6,96
		1,59	21,09	47,43	47,43	2,96	64,13	14,49	6,60

Table 16 : HPA-1 module (#3). Synthesis of power measurements with CW signal. Temp=[-20°C, 25°C, 90°C], Vd=40V & Vd=45V, Id=400mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

Temp (°C)	Biasing Point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
90	Vd=40V, Id=400mA	1,54	17,75	45,60	36,31	2,27	64,69	12,58	5,17
		1,57	17,75	45,69	37,07	2,32	62,56	12,61	5,14
		1,59	17,78	45,73	37,41	2,34	59,34	12,76	5,02
25	Vd=40V, Id=400mA	1,54	19,86	45,92	39,08	2,44	67,74	12,94	6,92
		1,57	19,84	45,97	39,54	2,47	67,61	13,49	6,35
		1,59	19,78	46,07	40,46	2,53	64,64	13,58	6,20
-20	Vd=40V, Id=400mA	1,54	20,94	46,06	40,36	2,52	68,88	13,53	7,41
		1,57	21,00	46,02	39,99	2,50	69,92	14,52	6,48
		1,59	20,94	45,99	39,72	2,48	68,93	13,98	6,96

Temp (°C)	Biasing Point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
90	Vd=45V, Id=400mA	1,54	18,31	46,51	44,77	2,80	64,15	12,98	5,33
		1,57	18,33	46,60	45,71	2,86	63,41	13,08	5,25
		1,59	18,27	46,64	46,13	2,88	60,30	13,16	5,11
25	Vd=45V, Id=400mA	1,54	20,18	46,78	47,64	2,98	65,91	13,29	6,89
		1,57	20,18	46,86	48,53	3,03	67,47	13,84	6,34
		1,59	20,16	46,84	48,31	3,02	64,98	14,38	5,78
25	Vd=45V, Id=400mA	1,54	21,23	46,82	48,08	3,01	65,80	13,81	7,42
		1,57	21,22	46,95	49,55	3,10	68,97	14,45	6,77
		1,59	21,19	46,99	50,00	3,13	67,26	14,99	6,20

Table 17 : HPA-1 module (#5). Synthesis of power measurements with CW signal. Temp=[-20°C, 25°C, 90°C], Vd=40V & Vd=45V, Id=400mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

HPA module-1 (#5) has been tested with different biasing point [100mA / 400mA / 800mA] and Temp=[25°C/90°C].

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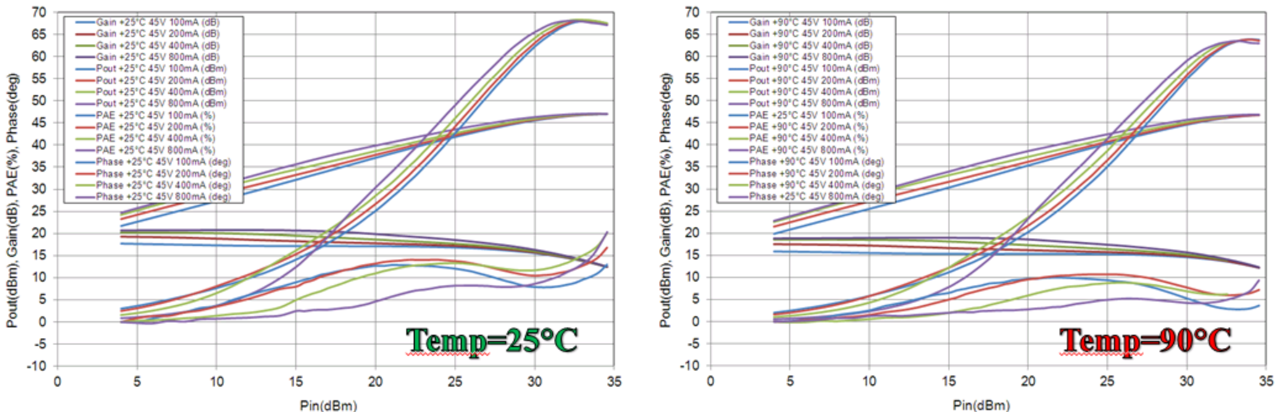

Figure 67 : HPA#1 module (#5). Power measurements with CW signal. Temp=[25°C, 90°C], Vd=45V, RF=1,5675GHz Id=[100mA/200mA/400mA/800mA]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

Synthesis of the results are presented in figure below. Biasing point has no impact on PAE performances. On the other hand, the selected biasing point will have an impact on gain compression and power density.

Temp (°C)	Frequency (GHz)	Drain Voltage (V)	Drain Current (mA)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	Max_PAE (%)	Gain (dB)	Compression (dB)
85	1,57	45	100	15,88	46,62	45,92	2,87	63,91	12,57	3,31
			200	17,52	46,67	46,45	2,90	63,83	12,63	4,89
			400	18,57	46,66	46,34	2,90	63,85	13,13	5,44
			800	18,82	46,72	46,99	2,94	63,53	13,69	5,13
25	1,57	45	100	17,72	46,89	48,87	3,05	68,04	13,34	4,38
			200	19,29	46,86	48,53	3,03	68,28	13,82	5,47
			400	20,24	46,94	49,43	3,09	68,31	13,90	6,34
			800	20,71	46,91	49,09	3,07	68,05	14,85	5,86

Figure 68 : HPA-1 module (#5). Synthesis of power measurements with CW signal. Temp=[25°C, 90°C], Vd=45V, RF=1,5675GHz Id=[100mA / 200mA / 400mA / 800mA]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

2.1.5.3 Multi-carrier mode power measurements. Run-1

In the following part, multicarrier measurements are presented. HPA-1 module (#5) has been tested with Vds=45V and different biasing point fixed in small signal (Ids=100mA / 200mA / 400mA / 800mA). Multi-carrier measurements have been performed at Temp=[-20°C, 25°C, 90°C].

The multicarrier signal characteristics are:

- 3000 carriers
- Span=40MHz
- Fc=1.5675GHz
- Notch: 1%

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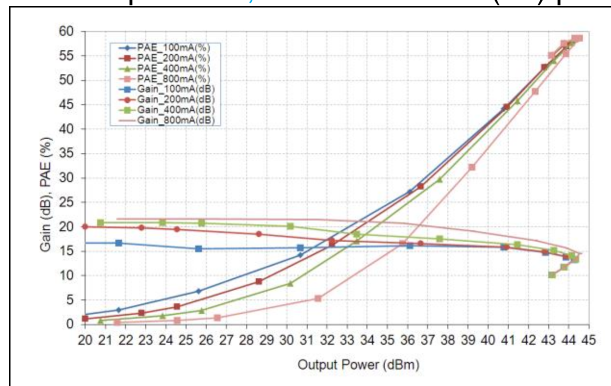
At Temp=-25°C, HPA-1 module (#5) power measurements are given versus Pout.



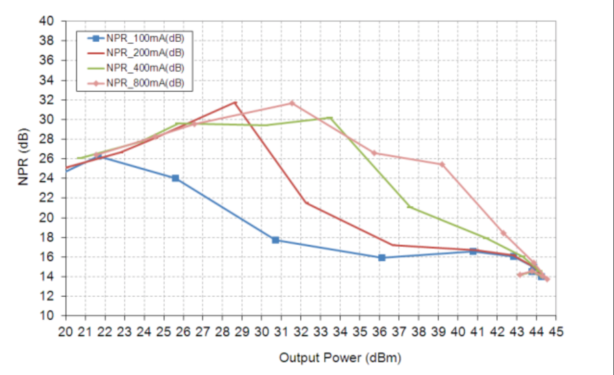


Figure 69 : HPA-1 module (#5) Power measurements with multi-carrier signal. Temp=-20°C. Vds=45V, RF=1,5675GHz, Span=40MHz, 3000 carriers, 1% notch. Gain(dB), PAE(%), NPR(dB) vs Pout(dBm)

At Temp=-25°C, HPA-1 module (#5) power measurements are given versus Pout.

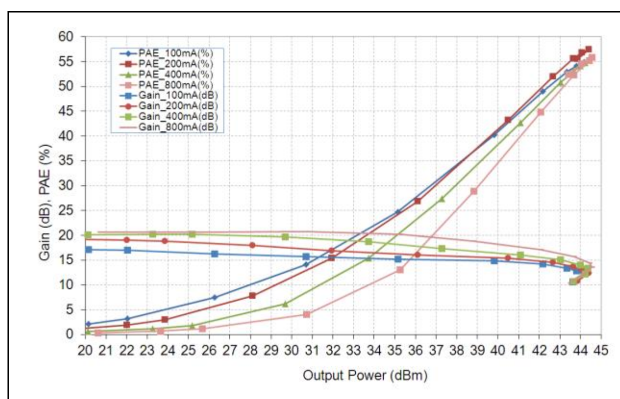
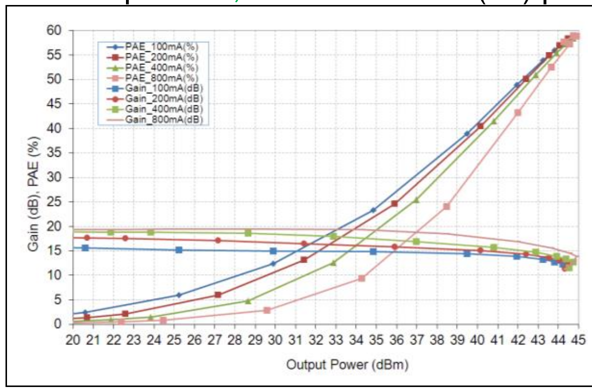


Figure 70 : HPA-1 module (#5). Power measurements with multi-carrier signal. Temp=+25°C. Vds=45V, RF=1,5675GHz, Span=40MHz, 3000 carriers, 1% notch. Gain(dB), PAE(%), NPR(dB) vs Pout(dBm)

At Temp=90°C, HPA-1 module (#5) power measurements are given versus Pout.



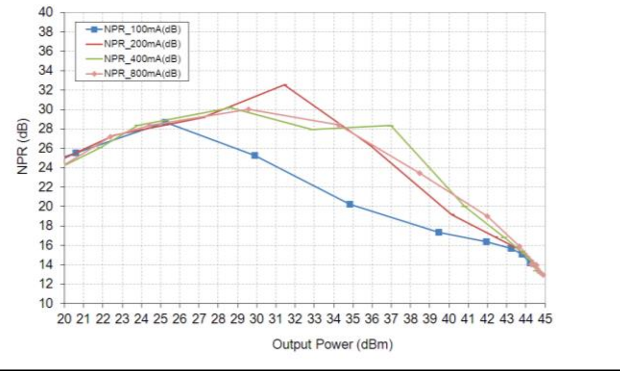


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Figure 71 : HPA-1 module (#5) Power measurements with multi-carrier signal. Temp=+90°C. Vds=45V, RF=1,5675GHz, Span=40MHz, 3000 carriers, 1% notch. Gain(dB), PAE(%), NPR(dB) vs Pout(dBm)

In the following table are summarized the main parameters measured during multi-carrier measurements : Pout and power density / NPR / PAE / Compression. This table will be used to select the best biasing point for the HPA module in order to achieve the RF performances in multi-carrier mode required at HPA level. In term of power density, the results are optimum with Ids=800mA. However, the gain compression is increased this representing a risk with respect to the reliability

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=100mA, Temp=-20°C	17,0	30,0	43,9	24,3	56,8	15,0	13,9	3,1
		31,0	44,3	26,7	58,1	14,0	13,3	3,7

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=200mA, Temp=-20°C	20,0	30,0	43,9	24,5	57,0	15,0	13,9	6,1
		31,0	44,3	26,9	58,3	14,0	13,3	6,7

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=400mA, Temp=-20°C	20,8	29,1	43,7	23,5	55,9	15,3	14,6	6,2
		31,0	44,3	27,2	58,6	14,0	13,3	7,5

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=800mA, Temp=-20°C	21,6	29,1	44,2	26,3	57,0	14,6	15,1	6,5
		31,0	44,3	27,0	58,7	14,1	13,3	8,3

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=100mA, Temp=25°C	17,6	31,0	43,8	24,0	54,2	15,0	12,8	4,8
		32,0	44,2	26,1	54,9	14,0	12,2	5,4

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=200mA, Temp=25°C	19,2	30,5	43,9	24,3	56,2	15,0	13,4	5,8
		31,5	44,2	26,5	57,2	14,2	12,7	6,5

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=400mA, Temp=25°C	20,1	30,0	44,0	25,0	54,1	15,0	14,0	6,1
		31,0	44,3	27,2	55,3	14,0	13,3	6,8

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=800mA, Temp=25°C	20,6	29,0	44,1	25,4	53,8	15,0	15,1	5,6
		30,0	44,4	27,7	55,2	14,0	14,4	6,2

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=100mA, Temp=90°C	15,9	31,0	43,8	24,0	56,0	15,1	12,8	3,1
		32,0	44,2	26,5	57,2	14,2	12,3	3,6

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=200mA, Temp=90°C	18,0	31,0	44,1	25,5	56,9	14,8	13,1	5,0
		32,0	44,5	28,1	58,3	13,9	12,5	5,5

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=400mA, Temp=90°C	18,9	30,0	43,9	24,7	55,5	15,2	13,9	5,0
		31,0	44,4	27,4	57,2	14,2	13,4	5,5

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=800mA, Temp=90°C	19,1	29,0	44,1	25,7	54,9	14,9	15,1	4,0
		30,0	44,6	28,5	57,2	14,0	14,6	4,6

Figure 72 : HPA-1 module (#5). Synthesis of power measurements with multi-carrier signal. Temp=[-20°C, +25°C, +90°C]. Vds=45V, RF=1,5675GHz, Span=40MHz, 3000 carriers, 1% notch. Id(A) and Ig(A) Pin(dBm)

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2.1.5.4 RF step measurements with multi-carrier signal : reliability of GH50-10 technology. Run-1

This paragraph summarizes the reliability test performed on GaN HPA L Band in the frame of the ARTES 5.1 ''SSPAs with European GaN Devices'' study. The goal of this reliability study is to define a Safe Operating Area through RF Multicarrier step stress (2 dB compression, 4 dB compression, 6 dB compression, 8 dB compression, 10 dB compression). For that, a dedicated multicarrier test bench have been developed.
Intermediate RF measurements and in situ monitoring are performed during this qualification.
Test plan is provided in the following table:

	Function	HPA 50 WATTS 16 mm
	Process	UMS GH50-10
	Frequency	1.56 GHz
	DC Bias	Vd=45V, Id = 100 mA (6,25 mA / mm)2 samples + 1 sample Id=400 mA (25 mA / mm)
DC Life test	Number of Sample	NA
	T° JUNCTION (Objective)	NA
	Electrical constraint	NA
	Duration	NA
RF Life test	Number of Sample	3 + 1
	T°	25°C
	DC Biases	Nominal DC biases
	Electrical Constraint	Multicarrier
		1 - Step stress :
		2 weeks / step from 4 dBc to 8 dBc
		2 - RF Life test :
		2000 hours @ XdBc - 2 dB or max PAE
	Monitoring	Gate, drain current, Input, output power
	Initial, Final & Intermediate Measurement	RF Characteristic : Pout, Gain, Id, Ig vs Pin, Phase vs input power

Table 18 : Test plan for RF step stress measurements of L-band GH50 HPA-1 module

3 samples have been tested during RF step stress with multicarrier signal:

- HPA-1 module (#2) = Sample n°2 = SN2
- HPA-1 module (#3) = Sample n°3 = SN3
- HPA-1 module (#5) = Sample n°5 = SN5

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Multi carrier signal is generated using white noise source. The « white noise » bandwidth is = 28 MHz. All the spike > 40 dBc outside the signal band width are eliminated. Synoptic and photographs of the multi-carrier test bench are provided in the following figures.

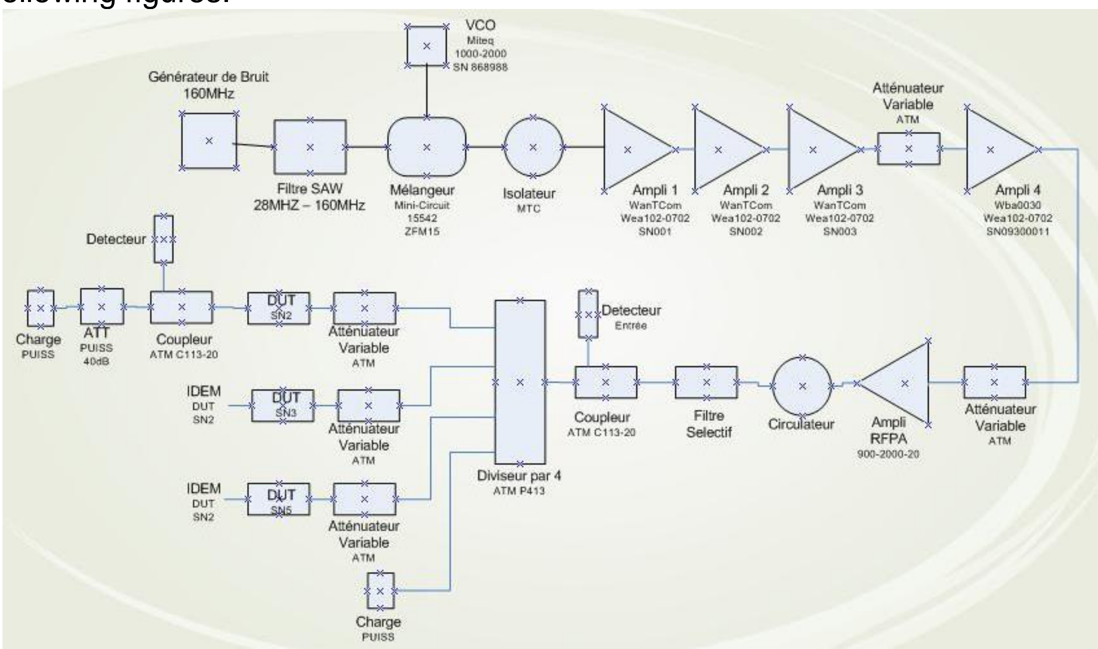

Figure 73 : Multi-carrier test bench

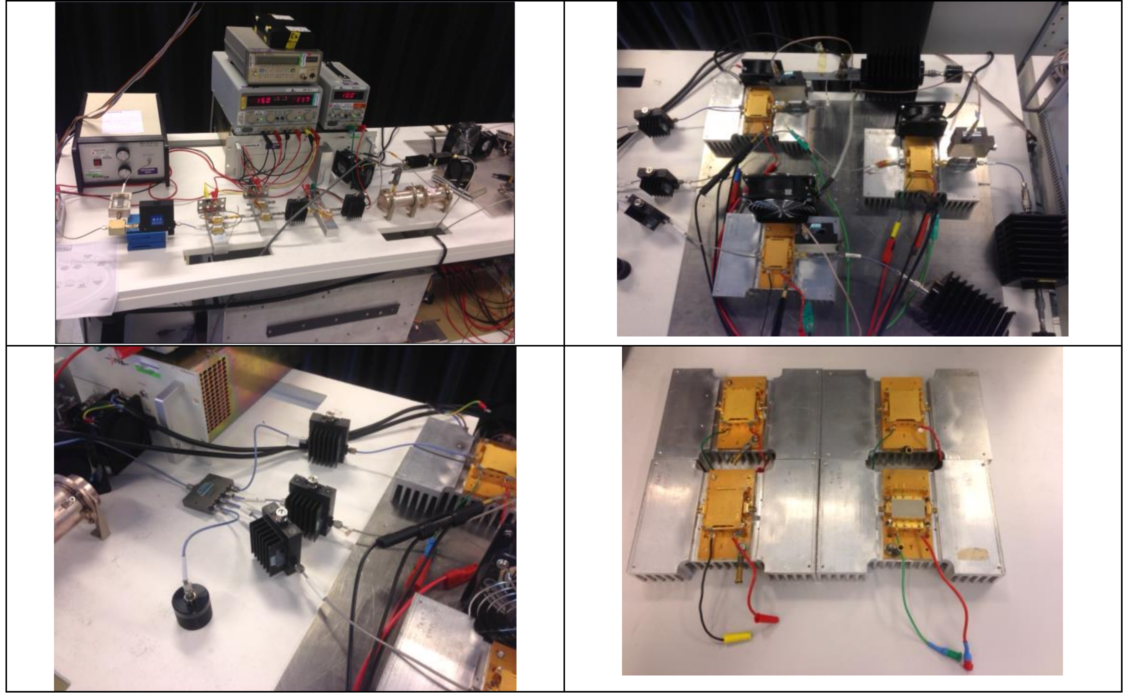

Figure 74 : Photographs of the multi-carrier test bench

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The figure here above describes the signal level respectively after the mixer, the amplifier 1, 2 ,3 and amplifier RFPA + filter

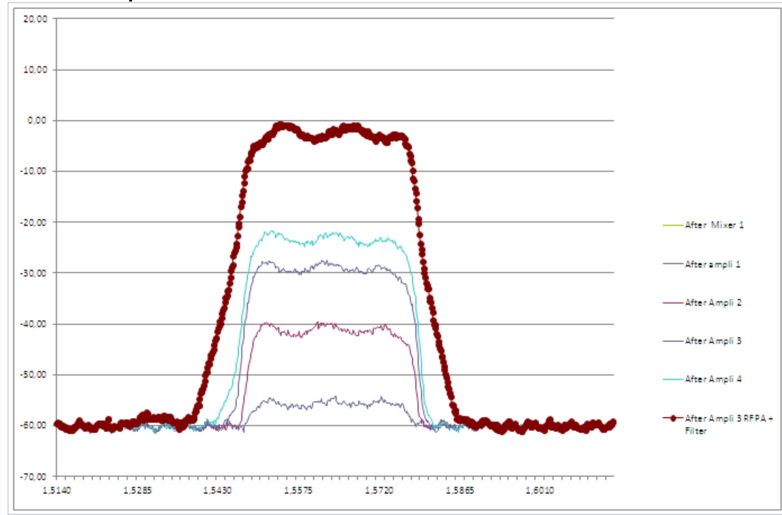

Figure 75 : Noise signal level at different point of the test bench

CCDF measurement (Complementary Cumulative Distribution Function) consist to analyze multi carrier signal in order to determine a probability that a phase recombination generate a signal higher than the average level signal.

Examples :

- For a CCDF = 1, we will have 1 spike / 10 000 = average level signal + 1 dB. (probability= 0.01%)
- For a CCDF = 9, we will have 1 spike / 10 000 = average level signal + 9 dB. (probability= 0.01%)

In the frame of this study, we need to obtain the highest value of CCDF. This value depends on the compression of the different amplifier. The more the compression is high, the more the value of the CCDF is low. The CCDF obtained is = 6.5 dB.

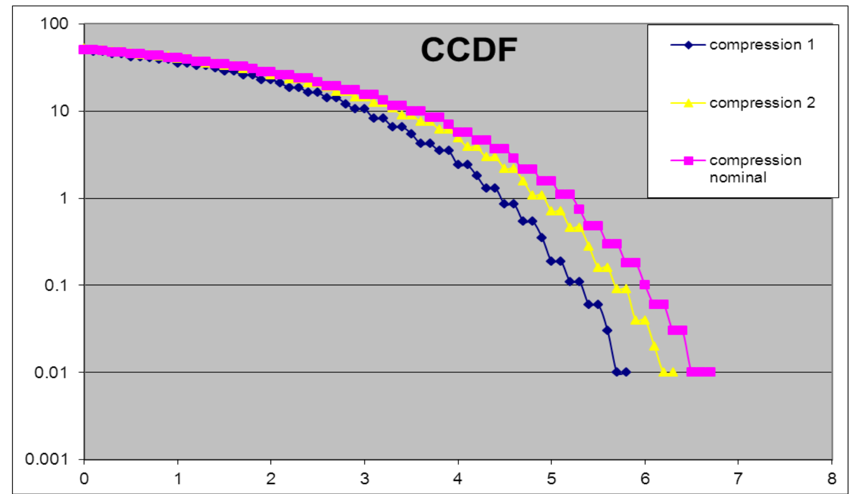

Figure 76 : CCDF Value for different compression values

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A dedicated test bench for initial, intermediate and final measurement bench is used for [S], AM/AM and AM/PM measurements after each step of compression (2 weeks / step from 4dBc to 8dBc). Synoptic and photographs of this test bench are provided in the following figures.

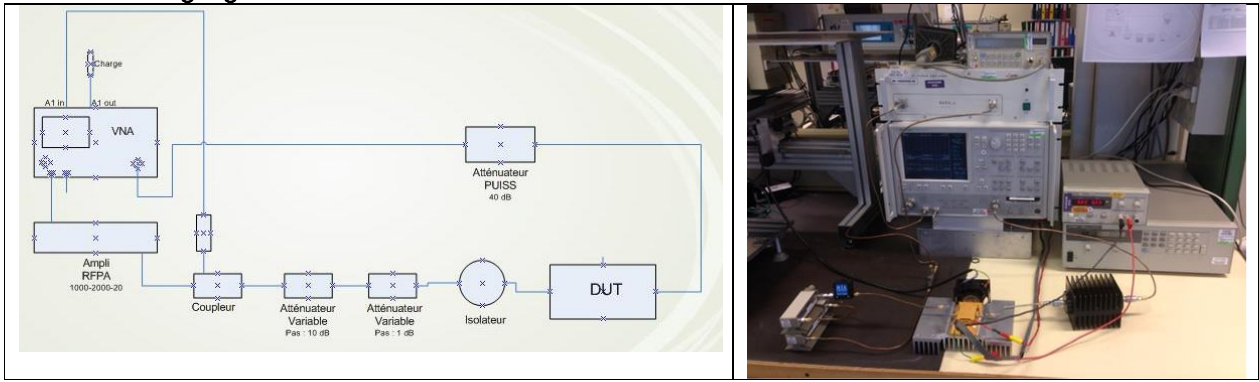

Figure 77 : Photography of the CW test bench for CW initial/intermediate and final measurements

Before starting the RF step stress campaign, initial characterization with the multicarrier signal have been performed in order to determine the non-linear characteristic of each samples. Example for HPA-1 module (#5) is given below:

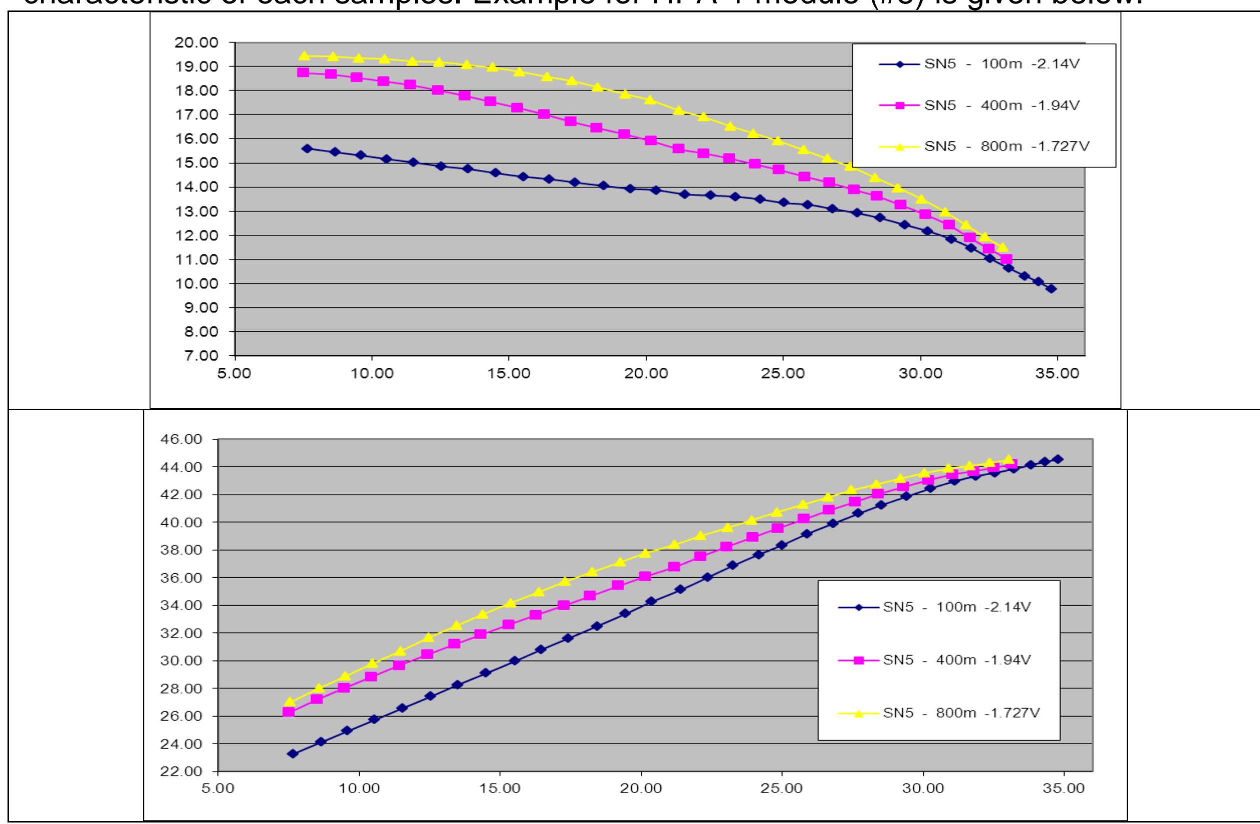

Figure 78 : RF step strep measurement: initial characterization of HPA-1 module (Sample n°5). Gain(dB) and Pout(dBm) versus Pin(dBm) for 3 different bias points: 45V/100mA & 45V/400mA 45V/800mA in small signal.

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In order to determine the power value during the in situ monitoring we use a detector. The power value versus the detected voltage is represented in the following graph.

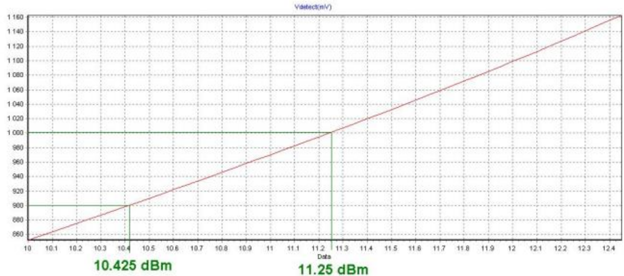

Figure 79 : Detector characterization : Detected voltage value (mV) versus power range(dBm)

The detector sensibility is : 0.825dB / 100mV that means 0.1dB / 12mV. This value must be applied for all the power in situ measurements. The detectors are used during power monitoring (input power and output power)

On three HPA-1 modules (#2, #3, [5), in Situ measurements have been continuously performed during steps @2dB, @4dB, 6dB, 8dB compression. The different parameters monitored are:

- Input power (dBm) and output power (dBm)
- Temperature (°C)
- Drain voltage (V) and Drain current (mA)
- Gate voltage (V) and gate current (mA)

An example of the in situ monitoring performed on HPA-1 module (#2) at Step 6dB compression is presented below:

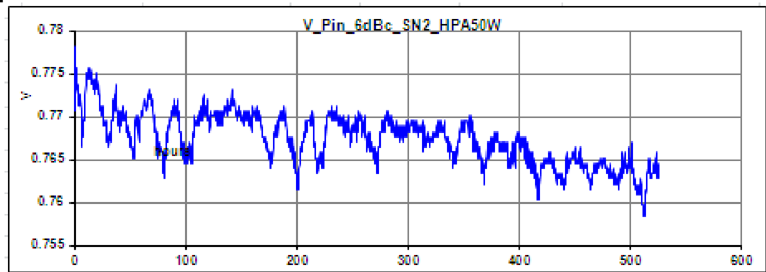

Figure 80 : HPA-1 module (#2). RF step stress measurement. Input power monitoring during 6dBc compression step

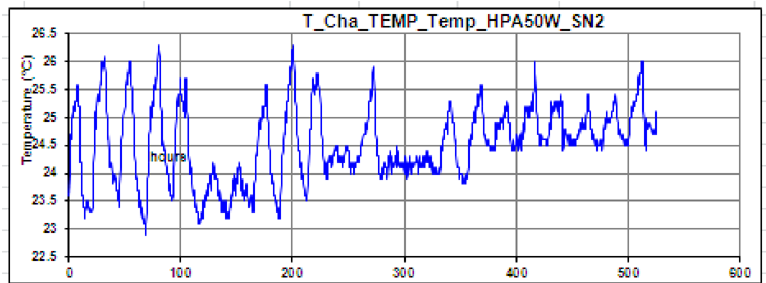

Figure 81 : HPA-1 module (#2). RF step stress measurement. Temperature monitoring during 6dBc compression step

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Figure 82 : HPA-1 module (#2). RF step stress measurement (6dBc step). Pout drift (detected voltage in V). Drain voltage drift(V). Drain current drift (mA). Gate voltage drift (V). Voltage current drift (mA)

For each HPA-1 module (#2, #3, #5), initial, intermediate and final have been performed. These measurements have consisted of:

- [S] parameters measurements

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- CW characterizations (AMAM and AMPM)
- Static measurements

Measurement data are presented for HPA-1 module #3 in the following graphs.
For the following graphs, the legend is:

- Et0 -> Initial measurements
- Et1 -> Measurements after step @ 2 dBc
- Et2 -> Measurements after step @ 4 dBc
- Et3 -> Measurements after step @ 6 dBc
- Et4 -> Measurements after step @ 8 dBc
- Et5 -> Measurements after step @ 10 dBc (for sample n° 3)

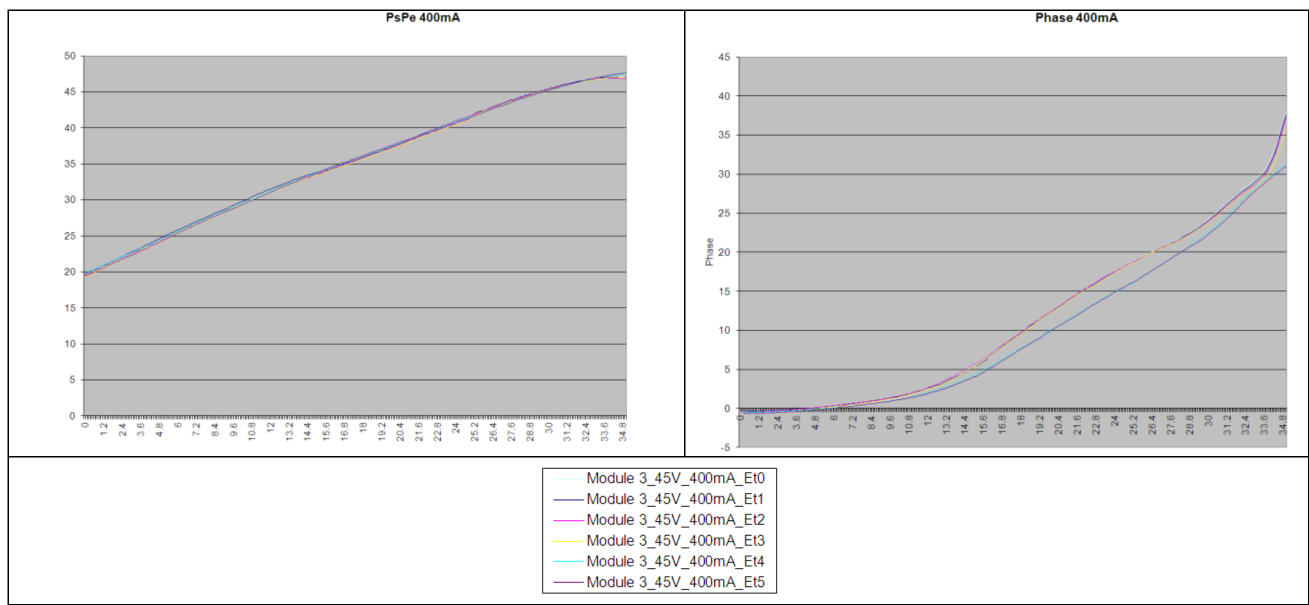

Figure 83 : HPA-1 module #3. AMAM and AMPM characterization in CW mode after each compression step of the RF step stress measurements

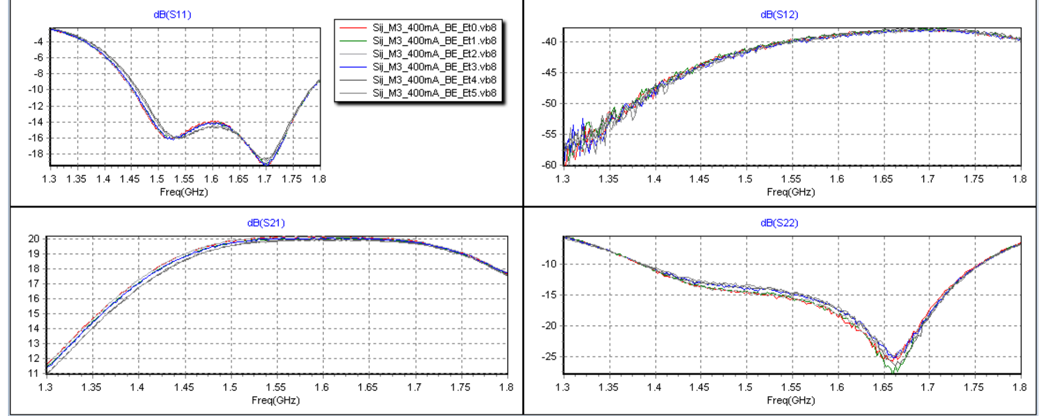

Figure 84 : HPA-1 module #3. [S] parameters measurements after each compression step of the RF step stress measurements

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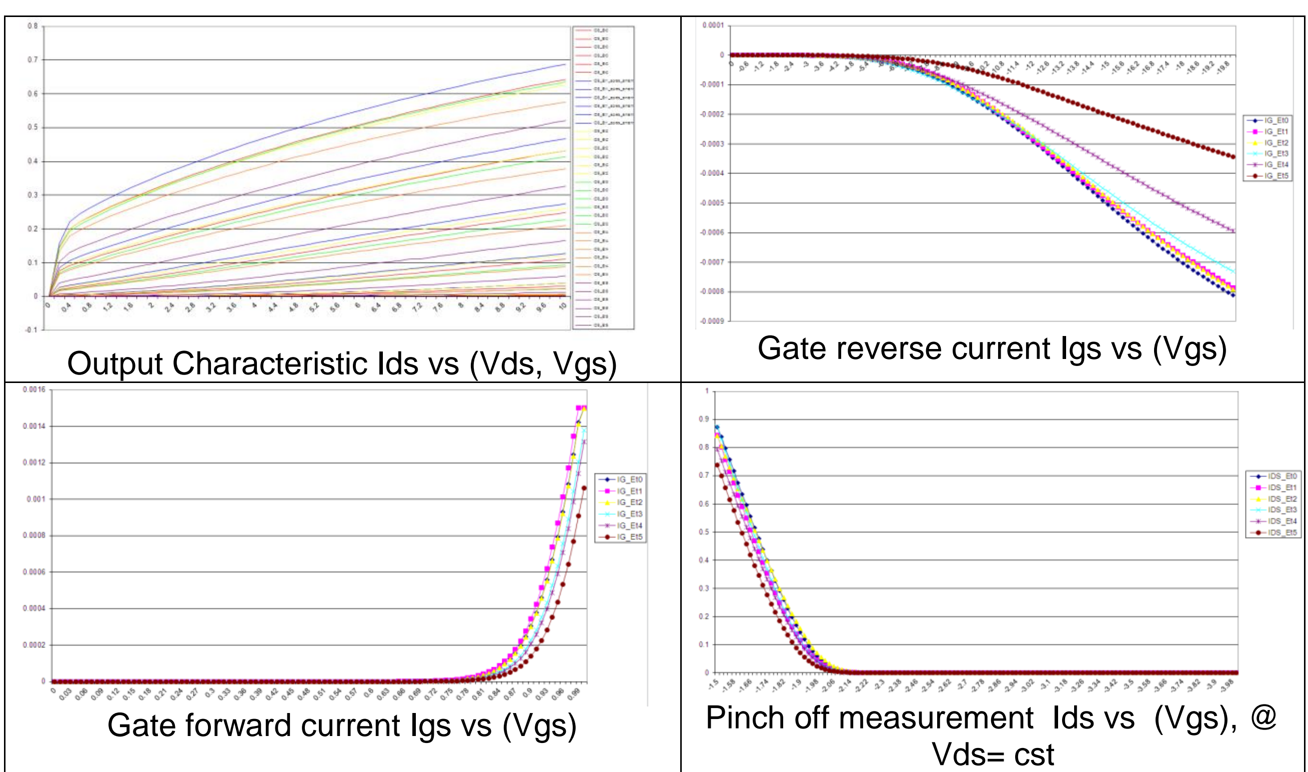

Output Characteristic Ids vs (Vds, Vgs)

Gate reverse current Igs vs (Vgs)

Gate forward current Igs vs (Vgs)

Pinch off measurement Ids vs (Vgs), @ Vds= cst

Figure 85 : HPA-1 module #3. Static measurements after each compression step of the RF step stress measurements

Regarding the compression parameter of 6,5dBc obtained at NPR=15dB: the RF step stress measurements have been performed up to 8dBc gain compression for two HPA modules and 10dBc gain compression for HPA#3 module. No degradation has been observed on dynamic performances, showing that high level of compression (6,5dBc) could be used.

2.2 Development of L-band hybrid GH50 HPA module (HPA-1 module): Phase 2

2.2.1 Reverse Engineering of HPA-1 module developed in Run-1

2.2.1.1 Back-simulations of HPA-1 module Run-1

Before presenting the detailed design of HPA-1 module (Run-2) , the following section summarizes the reverse engineering study of HPA-1 module (Run-1) designed during the phase 1 . Two methods have been used during the reverse engineering:

- Simulations based on a classical technique (Momentum simulation for passive networks and HFSS simulation for RF feed-through)
- Simulations based on advanced technique (full HFSS simulation)

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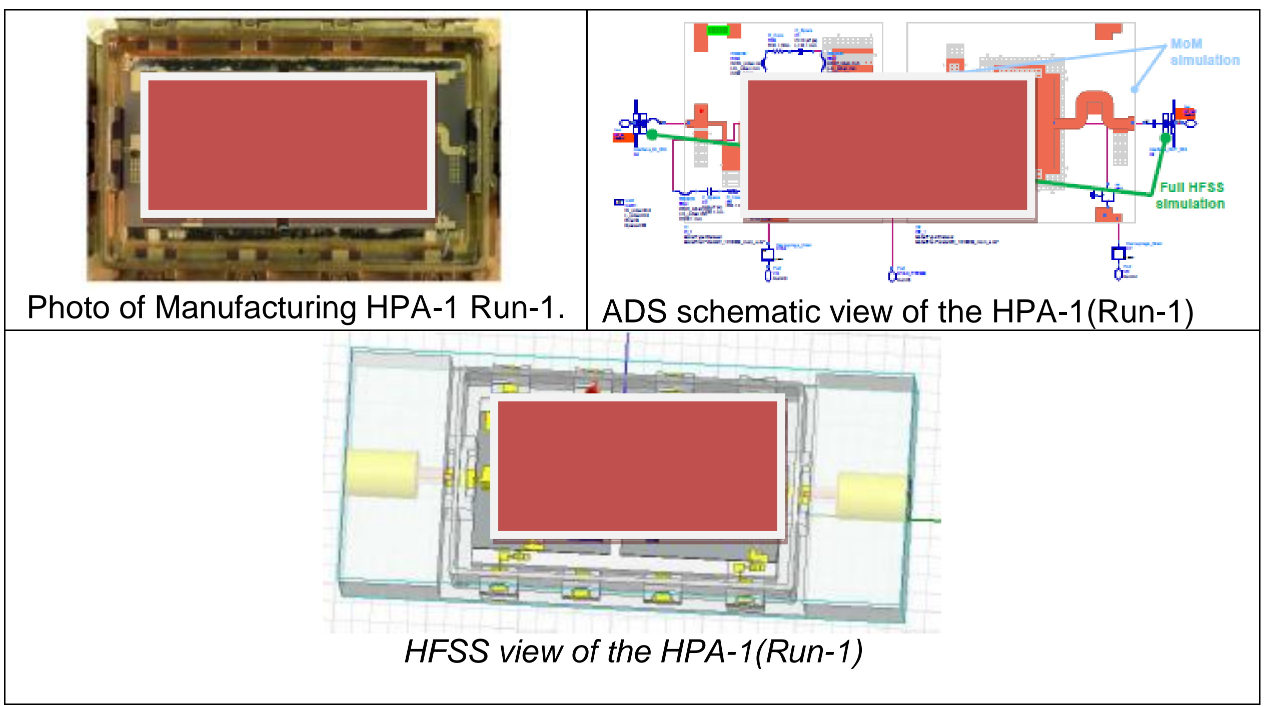

Photo of Manufacturing HPA-1 Run-1.

ADS schematic view of the HPA-1(Run-1)

HFSS view of the HPA-1(Run-1)

Figure 86 : Two methods used during the reverse engineering of HPA-1 module Run-1

The comparison of reverse engineering simulations are shown below

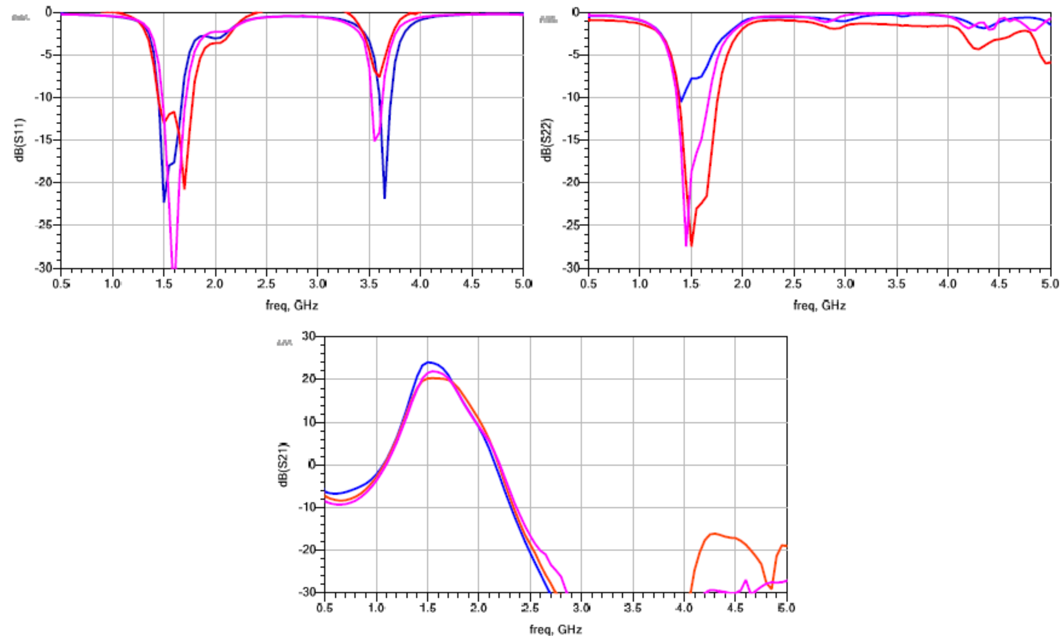

Figure 87 : HPA-1 module Run-1: S-parameter comparison of measurement and reverse engineering simulations

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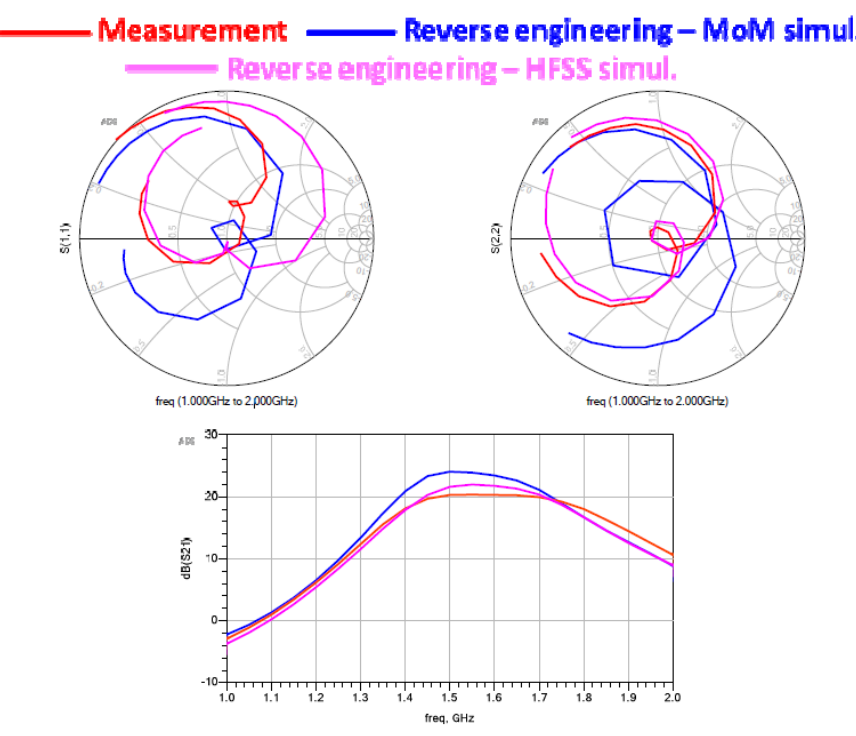

Figure 88 : HPA-1 module Run-1: S-parameter comparison zoom of measurement and reverse engineering simulations

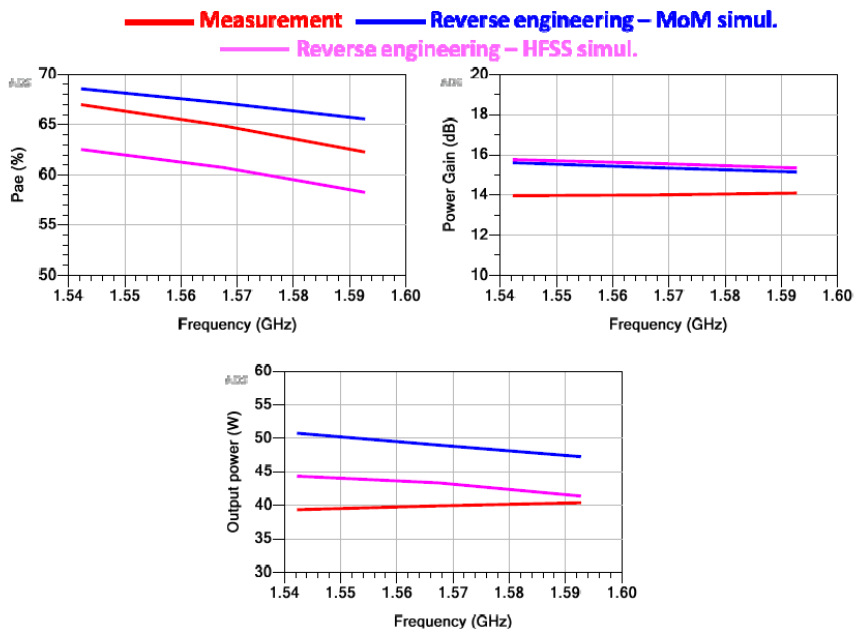

Figure 89 : HPA-1 module Run-1: HPA RF performance vs frequency comparison of measurement and reverse engineering simulations @ Pin=35dBm

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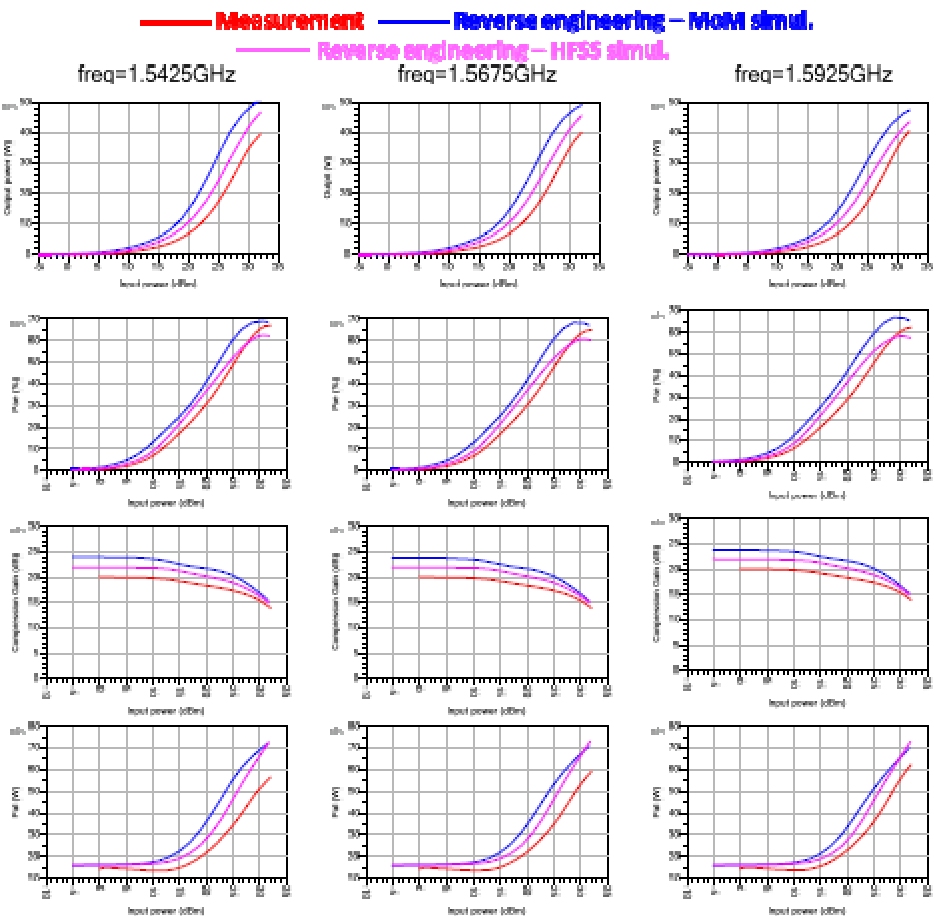

Figure 90 : HPA-1 module Run-1: HPA RF performance vs Pin comparison of measurement and reverse engineering simulations

In conclusion, in L-Band both MoM and HFSS simulation have similar behavior, but the HFSS simulation seems more realistic. Therefore, the design philosophy for the HPA design during phase is to obtained the RF performances with MoM simulation and the validation of such RF performance with HFSS simulations.

2.2.1.2 CCN on new specification for HPA-1 module

Through a CCN, TAS proposed to modify the center frequency from 1,5675GHz to 1,5385GHz. Indeed, this L-band HPA module is used as power stage of a new L-band GaN SSPA for MSS applications. The useful frequency range shall be [1,518-1,559 GHz] instead of [1,5425- 1,5925GHz]. This new equipment will be dedicated to the entire renewal market of constellations of mobile communications satellites. Thus, in phase 2, HPA-1 module are centered at 1.5385GHz.

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2.2.2 Manufacture and test the 0.5µm transistors and power-bars (GH50). Run-2

In the frame of the Phase 2 of “SSPA with European Gan Devices” contract, one 3GH50-10 wafer has been manufactured by UMS. For this run, one specific mask-set, named “STARDUST”, was developed in collaboration with TAS-F. UMS was in charge of wafer manufacturing, on wafer tests and delivery. This paragraph report summarizes on-wafer measurements carried out on the Stardust wafer, referenced S355015/1R036. The workflow is as follows:

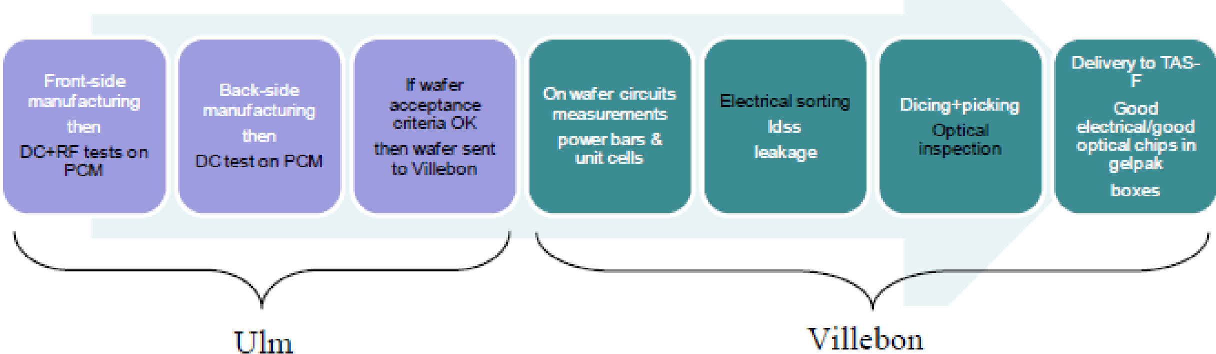

Figure 91 : UMS workflow for the manufacturing & test of GH50 maskset (Run-2)

Tile composition and dimension are presented in the following figure

Y / X	3,38	4,09	0,85	1,41
1,05	PCM1	PCM3	2,4mm: 8x300µm Pitch 50µm	PCM5
0,85	2cells 2,4mm (2x8x150µm) Pitch70µm	9,6mm: 8x8x150µm Pitch 70µm	1,2mm: 8x150µm Pitch 70µm	2,4mm: 2x8x150µm Pitch 70µm
0,85	9,6mm: 8x8x150µm Pitch 50µm	9,6mm: 8x8x150µm Pitch 70µm	1,2mm: 8x150µm Pitch 50µm	2,4mm: 2x8x150µm Pitch 50µm
0,85	9,6mm: 8x8x150µm Pitch 50µm	12mm: 8x10x150µm Pitch 50µm	1,5mm: 10x150µm Pitch 50µm	3mm: 2x10x150µm Pitch 50µm
0,85	9,6mm: 8x8x150µm Pitch 50µm	12mm: 8x10x150µm Pitch 50µm	1,5mm: 10x150µm Pitch 50µm	3mm: 2x10x150µm Pitch 50µm
1,05	11,8mm: 8x8x185µm Pitch 50µm	11.8mm: 8x8x185µm Pitch 70µm	1,48mm: 8x185µm Pitch 70µm	1,48mm: 8x185µm Pitch 50µm
1,1	25,6mm: 8x8x400µm Pitch 50µm	32mm: 8x10x400µm Pitch 50µm	4mm: 10x400µm Pitch 50µm	8mm: 2x10x400µm Pitch 50µm
1,05	11,8mm: 8x8x185µm Pitch 50µm	20mm: 8x10x250µm Pitch 50µm	2,5mm: 10x250µm Pitch 50µm	5mm: 2x10x250µm Pitch 50µm
1,05	19,2mm: 8x8x300µm Pitch 50µm	16mm: 8x8x250µm Pitch 70µm	2mm: 8x250µm Pitch 70µm	4mm: 2x8x250µm Pitch 70µm
1,05	11,8mm: 8x8x185µm Pitch 50µm	11.8mm: 8x8x185µm Pitch 70µm	3mm: 10x300µm Pitch 50µm	2,96mm: 2x8x185µm Pitch 50µm
1,05	19,2mm: 8x8x300µm Pitch 50µm	24mm: 8x10x300µm Pitch 50µm	2,4mm: 8x300µm Pitch 50µm	6mm: 2x10x300µm Pitch 50µm
1,05	19,2mm: 8x8x300µm Pitch 50µm	12mm input H2 matching: 8x10x150µm Pitch 50µm	1,5mm 10x150µm Pitch 50µm H2 input matching	PCM6

Figure 92 : Stardust Tile composition

In the case of the Stardust wafer 1R036 (Run-2), as well as Sabrina wafer in 2011 (Run-1), we can notice that all the parameters concerning the PCM are well centered. As regards to the PCM parameters both Run-1 and Run-2 exhibit very close features.

Some layouts of the power unit cell integrated into the Stardust wafer are presented below:

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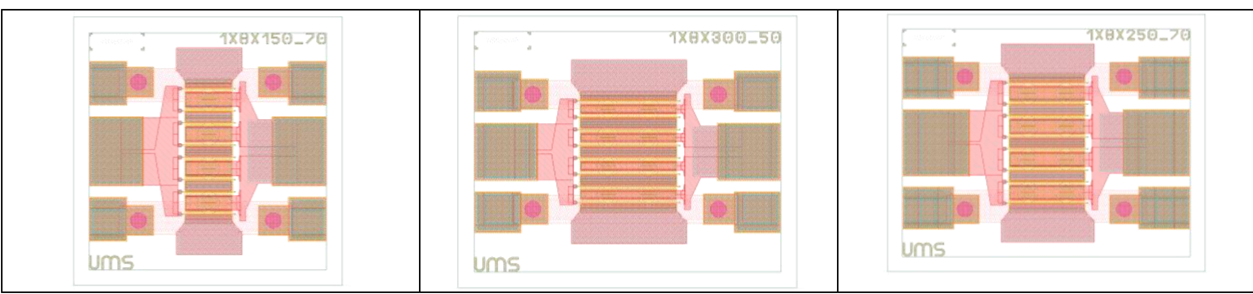

Regarding the power unit cells, S parameter measurements were carried out on the full wafer map for all the test cells. The measurements conditions were as follows:

- Frequency range : 0.5-21GHz
- Frequency step : 250MHz
- Biasing points :Id=50mA/mm Vd=10-20-40V

As example for the 8x250µm unit cell, the maximum stable gain /maximum available gain is plotted on the following graphs for the highest drain voltage bias point Vds=40V. We can notice the good homogeneity chip to chip.

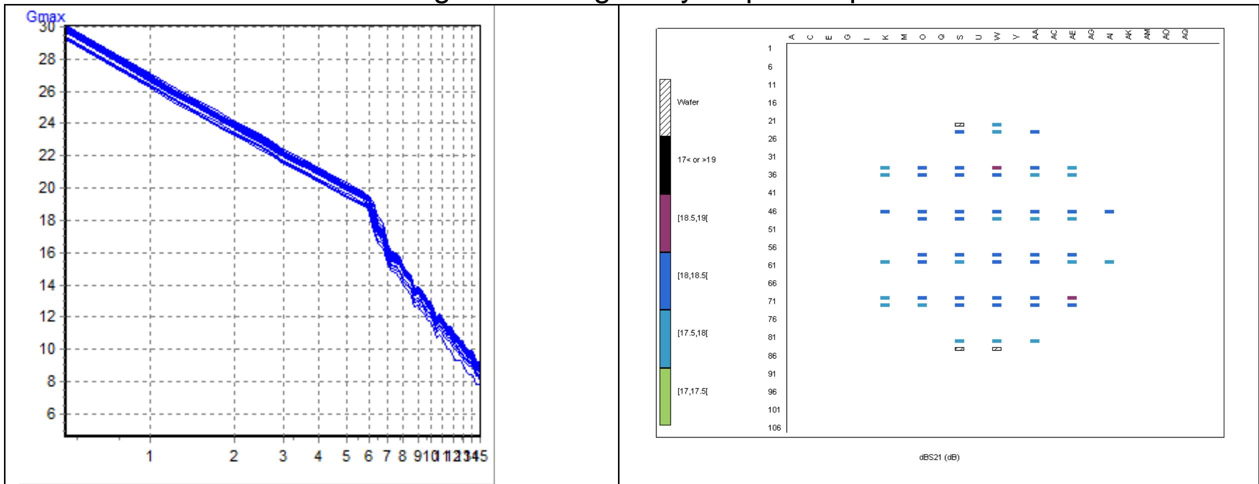

Figure 93 : 8x250_70 Vd=40V Id=50mA/mm. S21 parameter mapping at 40V&Id=50mA/mm

Specific load-pull measurements have been carried out in order to get more information about the large signal performance homogeneity on a whole wafer. Measurements have been carried out at 4Ghz on three topologies: 1x8x150_50, 1x8x150_70 and 1x8x250_70

For each topology, about 30 samples have been tested on the Stardust wafer S355015/1R036. The next graphs show for 8x250µm unit cell the performance homogeneity we could expect at transistor level matched with fixed loads at the input and the output. The output impedances at fundamental frequency and second harmonics have been chosen for maximizing PAE.

The impedances are set up to:

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- Gsource@fo=0.7/165.1°
- Gload@fo=0.59/97.9°
- Gload@2fo=0.8/90°
- Gload@3f0=0.0

Power sweep@4GHz for 8x250_70 transistor	Output power wafer mapping at 5dB compression for 8x250_70 transistor
Mask : STARDUST, Lot : S355015, Wafer : 1, Device : 1X8X250_70 Output power distribution for 8x250_70 transistor	Power Added Efficiency for 8x250_70 transistor

Figure 94 : On-wafer loadpull measurement of 8x250µm power cell unit

Some layouts of the power unit cell integrated into the Stardust wafer are presented below

- 8x8x250_70: Xwith dicing street=4.19mm Ywith dicing street=1.15mm

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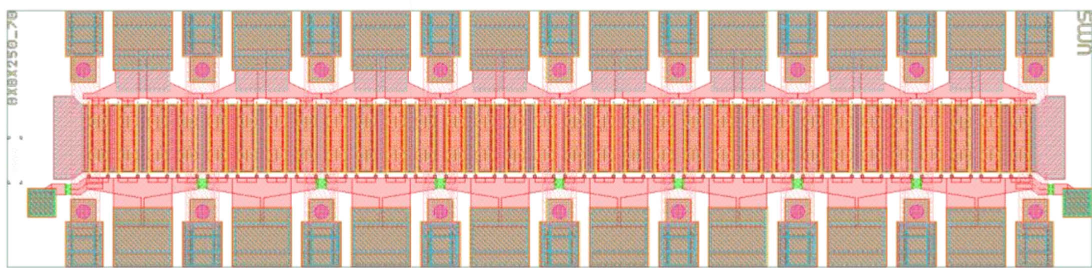
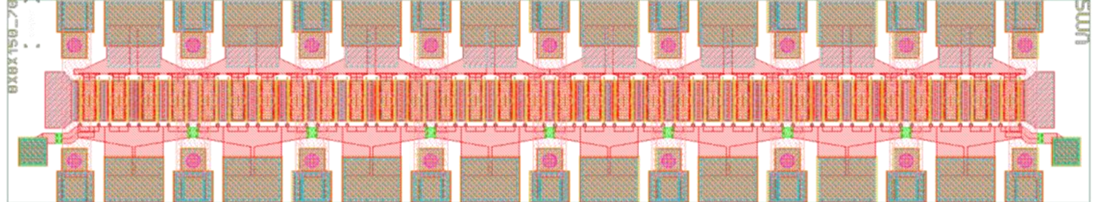
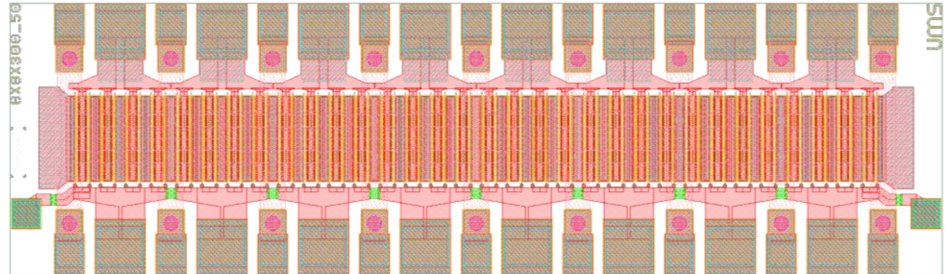


- 8x8x150_70: Xwith dicing street=4.19mm Ywith dicing street=0.95mm



- 8x8x300_50: Xwith dicing street=3.48mm Ywith dicing street=1.15mm



These Power bars are measured in DC mode thanks to specific probe card, more. All signal pads are connected together as well as ground pads through the probes card.
The screening procedure applied on every power bar of the whole wafer is:

- Schottky diode: A gate voltage swing is applied on the power bar with an open circuit on the drain. The gate current is measured. This enables to check the behaviour of the gate- source schottky diode. The results are gathered per power bar topology.
- Saturated drain current: Saturated drain current is measured in pulse mode for thermal issue. The biasing conditions are Vgs=0V and Vds=10V. On the next graphs we can look at the saturated drain current mapping for each power bar topology.
- Pinch-off voltage: During this measurement, a current loop looks for Idss/100, and then the associated gate voltage is defined as the “pinch-off voltage”. All the results are summarized in two charts. One is depicted the Vp spread per topology.
- Gate/drain current leakage: a leakage test is performed; the power bars are pinched-off under -7v with an associated drain voltage of 40V. The gate and drain currents are measured.
- were measured on every power bar of the whole wafer.

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Measured performance of 8x8x250µm power-bar are presented below.

Schottky diode measurements

Saturated drain current measurements

Trend chart for Saturated drain current

Trend chart for Pinch off voltage

Trend chart for Drain leakage

Figure 95 : 8x8x250µm power-bar on-wafer measurements

The PCM data have shown that this Stardust wafer is in agreement with the 3-GH50-10 technology acceptance criteria. On–wafer electrical characterizations have been

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carried out on all the devices. All transistors and power bars have been tested. Power bars have been tested following the UMS standard “screening procedure” for GaN devices. All the tests performed, S parameter, load-pull and DC screening have shown a very good homogeneity of the performance whatever the devices location on the wafer. As a results, the electrical yield should be very good.

2.2.3 Characterization and modeling of the 0,5µm transistors and power-bars. Run-2

2.2.3.1 Unitary cell measurements. Run-2

This paragraph gathers AMCAD Engineering and XLIM tasks achieved within the framework of the ARTES 5.1 SSPAs with European GaN Devices, Phase2 (Run-2). For unitary cell, AMCAD Engineering tasks consisted in pulsed I(V) with pulsed [S] measurements, load pull measurements and devices modeling. For power bar, AMCAD Engineering tasks consisted in load pull measurements. For power bar model, update of the model has been performed by AMCAD based on load-pull measurements.

The system set up for the transistor (8x250µm UMS) characterization is described below. The bias voltages and S-parameters are performed in CW mode.

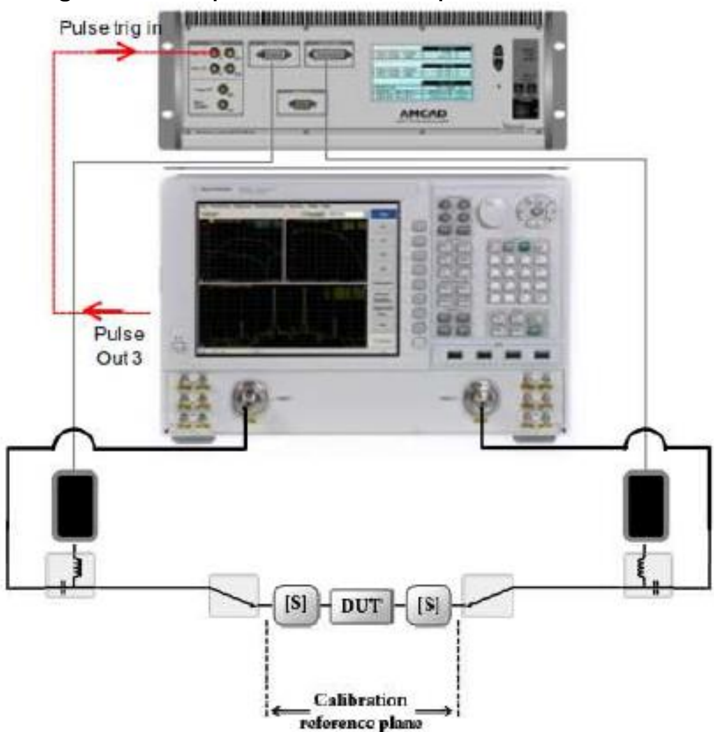

Figure 96 : AMCAD I(V) and [S] test bench for transistors characterizations. Run-2

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The principle of pulsed measurement is to describe the I(V) network by quasi-isothermal measurements using short pulses around a quiescent bias point selected. The quiescent bias point of rest is provided by the voltage levels and Vgs0 vds0. This results in a current Ids0 polarization. Pulses, whose levels are represented by VGSI, IGSI, VDSI IDSI and describe all the characteristics of input and output of the transistors. Principle of the S-parameters measurements in pulse mode is the same than the one used in Phase 1 (Figure 17)

5 samples are supplied by UMS:
-> Ref: W81, W69, AA33, AA57, AA45

Preliminary pulsed I(V)/RF measurements have been performed on each sample of order to estimate the process dispersion and to select the most representative samples for the complete characterizations. These dispersive measurements have been performed at ambient temperature (25°C). The results for the different transistor are shown hereafter.

Maximum gain (dB)

Maximum gain (dB)
Frequency (GHz)
IV_SP_DC_Sample_AA33.mes
IV_SP_DC_Sample_AA45.mes
IV_SP_DC_Sample_AA57.mes
IV_SP_DC_Sample_W69.mes
IV_SP_DC_Sample_W81.mes

Maximum gain (dB)

Maximum gain (dB)
Frequency (GHz)
AA57 - f = 1.5385 GHz X: 1.539, Y: 25.8
AA33 - f = 1.5385 GHz X: 1.539, Y: 25.78
W69 - f = 1.5385 GHz X: 1.539, Y: 25.77
W81 - f = 1.5385 GHz X: 1.539, Y: 25.64
AA45 - f = 1.5385 GHz X: 1.539, Y: 25.62
IV_SP_DC_Sample_AA33.mes
IV_SP_DC_Sample_AA45.mes
IV_SP_DC_Sample_AA57.mes
IV_SP_DC_Sample_W69.mes
IV_SP_DC_Sample_W81.mes

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Figure 97 : Dispersive [S] measurements on transistors 8x250µm GH50. Run-2 (bias points corresponding to surrounded points on the I(V) curves, Vds=40V)

The representative samples chosen are referred W81. Measurements with temperature have been performed at 25°C, 60°C and 90°C. The results obtained are shown hereafter.

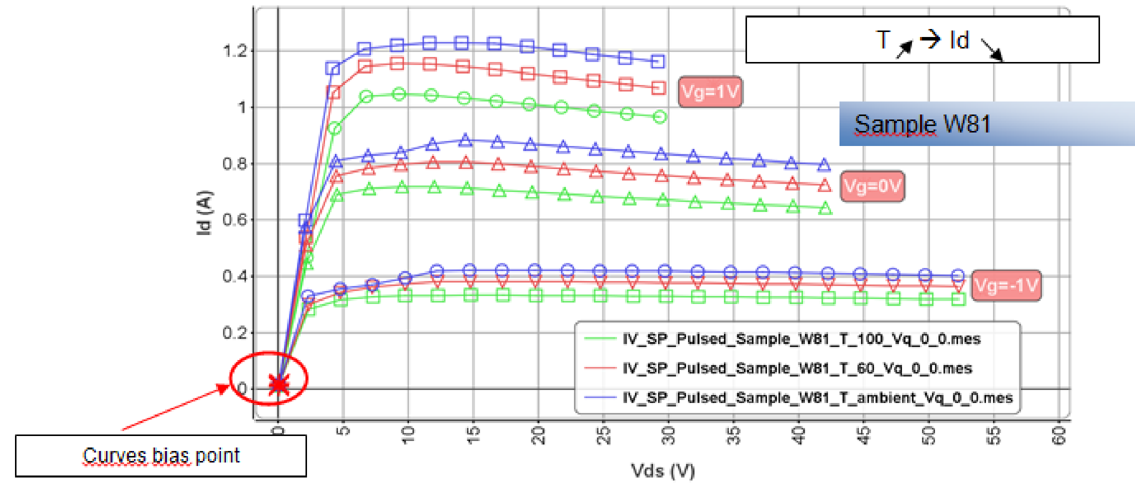

Figure 98 : Output current with different chuck temperature (25°C, 60°C, 100°C) Transistor 8x250µm Sample W81 measurements. Run-2

Idss is reduced by 8% to a rise of 75 ° C the chuck temperature.

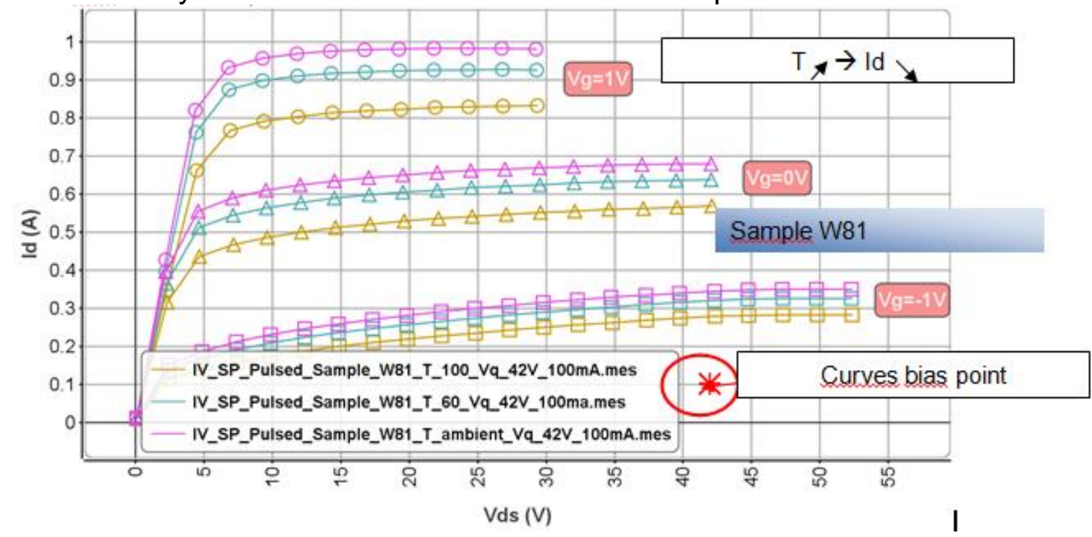

Figure 99 : Output current with different chuck temperature (25°C, 60°C,100°C), transistor 8x250µm GH50 measurements (bias points Vds0=42V, Ids0=100mA)

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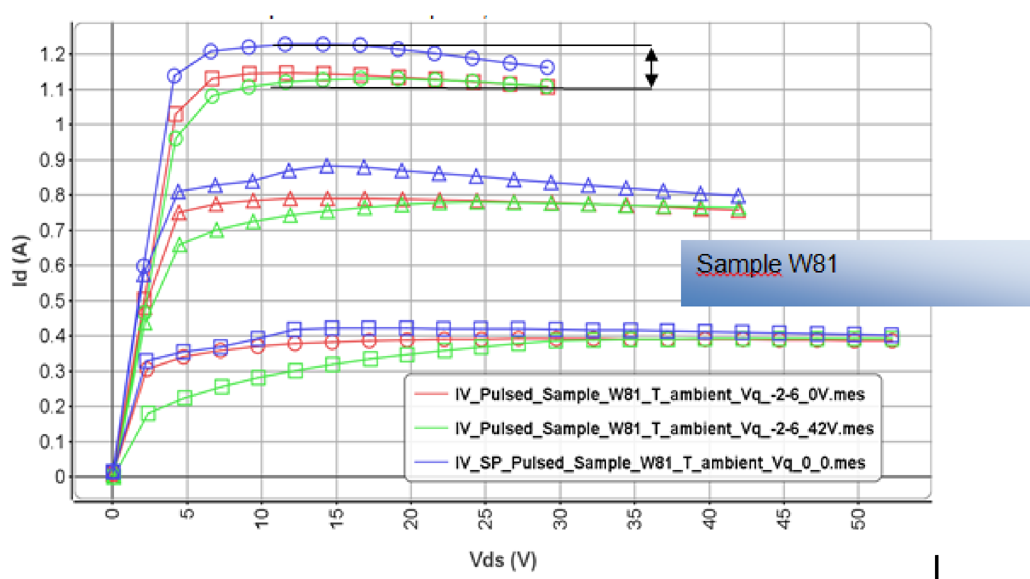

Figure 100 : Highlighted phenomena traps

The effect on the output characteristic is a reduction of the drain current of 8%

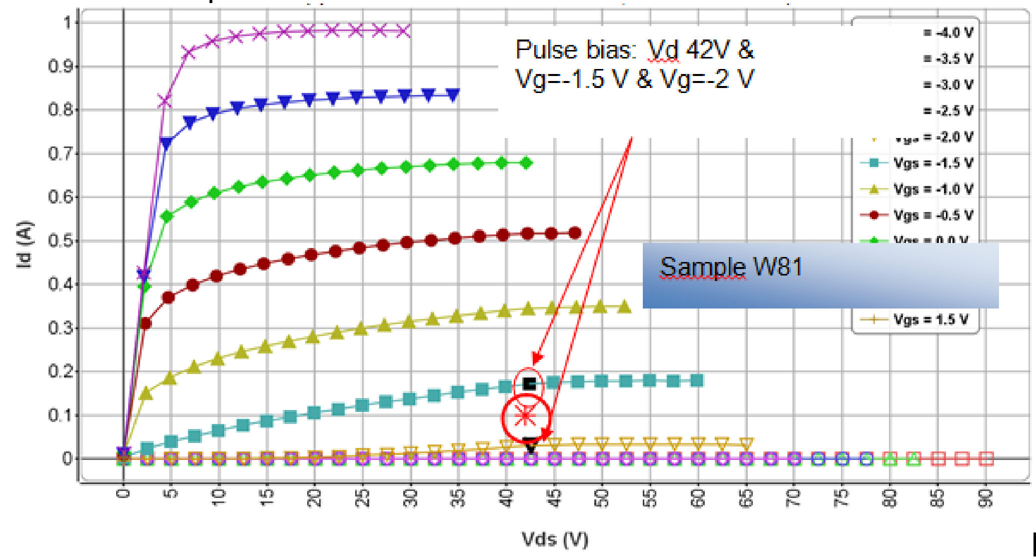

Figure 101: Output current, quiescent bias: (42V, 100mA), (chuck temperature = 25°C), transistor 8x250µm GH50

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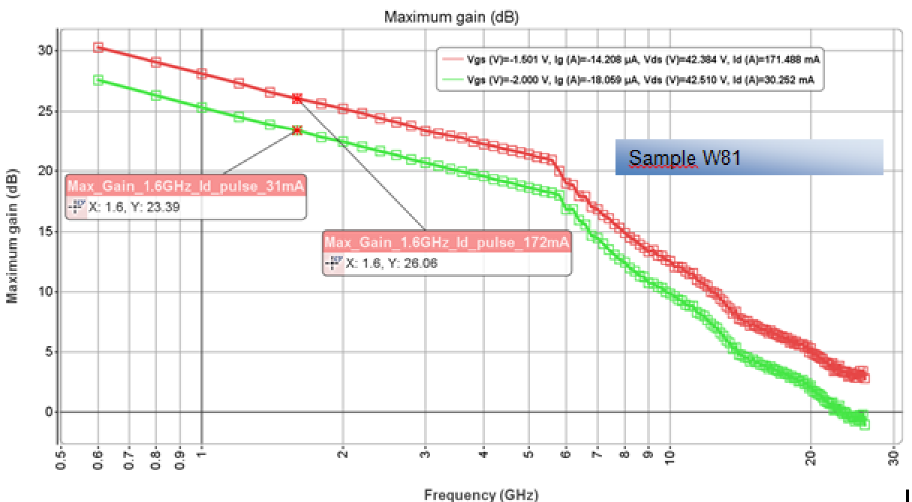

Figure 102 : Maximum Gain @ Vds0=40V, Ids0=50mA/mm

Load Pull measurements were performed in CW mode at a 1.5385GHz. The impedances were optimized at the fundamental frequency and the harmonics 2 and 3. The system set up for the devices characterization is the same used in phase 1 (Figure 23).

The objective is to find the optimal impedances in order to have the best power added efficiency (PAE) for f0 = 1.5385GHz CW mode. Load Impedance harmonic 2f0 is also optimized to achieve maximum PAE. It is optimized in active mode. Source impedance f0 is optimized to find the best Pin for a similar Psource.Source impedance harmonic 2 f0 is also optimized to achieve maximum PAE. It is optimized in active mode.

The 8x250µm components are polarized in DC mode:

- Vds0=42V, Ids0= 50mA/mm

The reference sample W81 is the selected transistor to realize the study. Several samples will be used to validate end optimization measures and study the dispersion.

The load-pull Optimization methodology used during this campaign is:

- Optimization of f0 load impedance: A first optimization of the load impedance is made at low level to determine the optimal impedance zone when the transistor operates in the linear regime. For this impedance, a power sweep is then performed in order to observe the performance obtained. The power that provides the maximum added power efficiency is raised to perform a second optimization of the load impedance (nonlinear regime). During these optimizations, the load impedances at 2f0 and 3f0 are equal to 50 ohms. During these first measures it appeared that the transistors are conditionally stable, this was confirmed by S-parameter measurements (measurements made on 50Ohms support and source). These Sparameter measurements give a good indication of the places of the Smith chart for which the transistor may be unstable. For Γload@f0=0.483, 50.5°, transistor reaches a 66.08% PAE.

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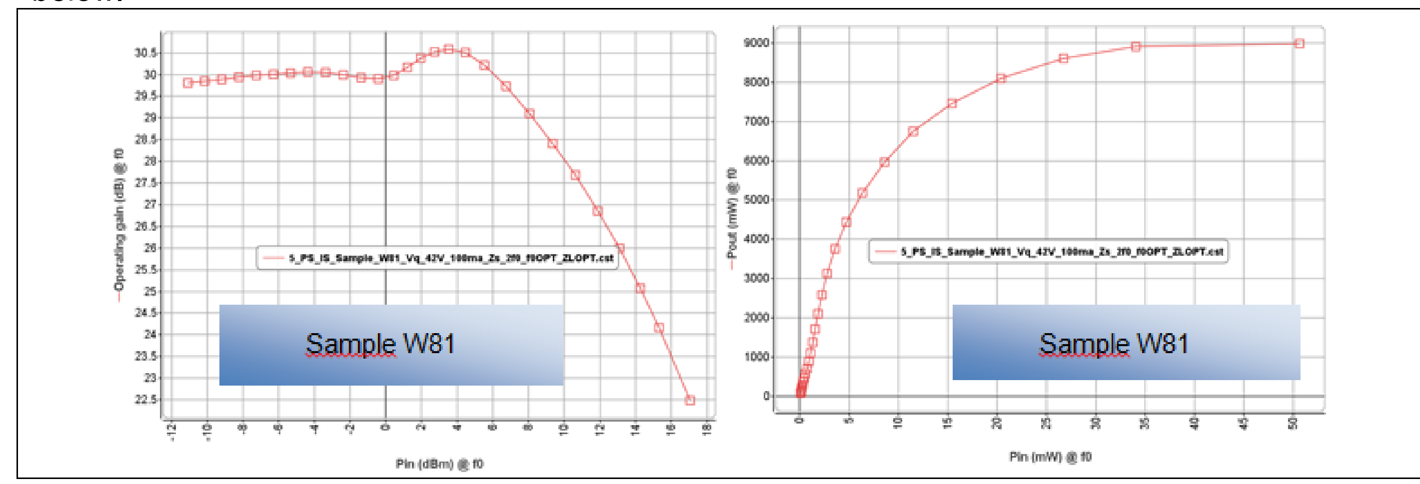
- Optimization of 2f0 load impedance: the load impedance at f0 is now set to the optimum impedance PAE. An impedance sweep at 2f0 is now performed to a input power level within the transistor to obtain the maximum PAE. The impedance at 3f0 remains at 50Ohms. For Γload@2f0=0.986/44.99°, transistor reaches a 76.36% PAE. (10 points increasing).
- New optimization of the f0 load impedance: With this new optimization of f0 load impedance, the PAE reaches 79.66% (4 pts increasing, 2f0 load impedance is fixed on its optimal).
- Measurement and optimization of f0 Source. Source impedance f0 is optimized to find the best Pin for a similar Psource. Zsource@2f0 is set to 50Ω, Zload@f0&2f0 are set to PAE optimum (Γload@f0=0.599/44.61°, Γload@2f0= 0.986/44.99°). We obtain a maximum Pin for Γsource@f0=0.801/141.7°, Pin reaches a 17.33 dBm for 18.27dBm of Psource, the PAE reaches 82% (2,5 points increasing)
- Optimization of 2f0 source impedance. For this optimization, source impedance 2f0 is optimized. Γload@f0&2f0 are set to PAE optimum (Γload@f0=0.599/44.61°, Γload@2f0=0.986/44.99°) and Γsource@f0 is set to Pin optimum Γsource@f0=0.801/141.7°. For Γsource@2f0=0.845/14.9°, the PAE reaches 82.4%. The 2f0 source impedance doesn't permit to increase the PAE.

The performances obtained for these optimal PAE load impedances are depicted below.



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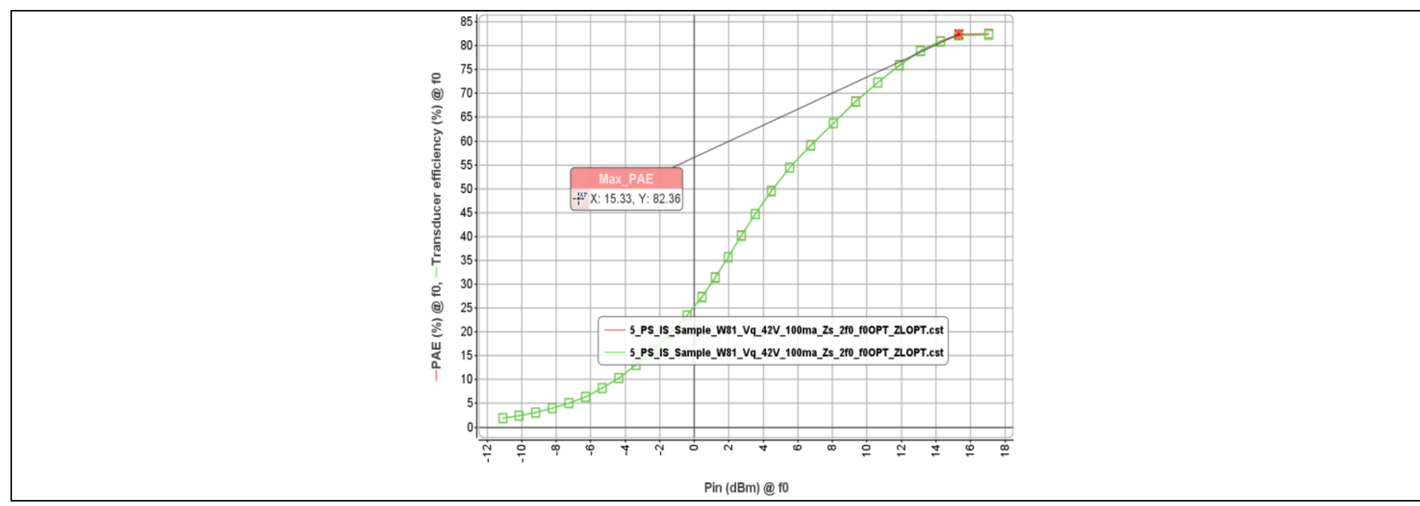

Figure 103 : Pout / PAE / Gain vs Pin after loadpull optimization. Optimized load (H1, H2) for optimal PAE performance. Vds=42V, 50mA/mm.

Regarding the RF performance vs Technology Dispersion, the load impedances are substantially similar to the fundamental frequency and harmonic frequency.

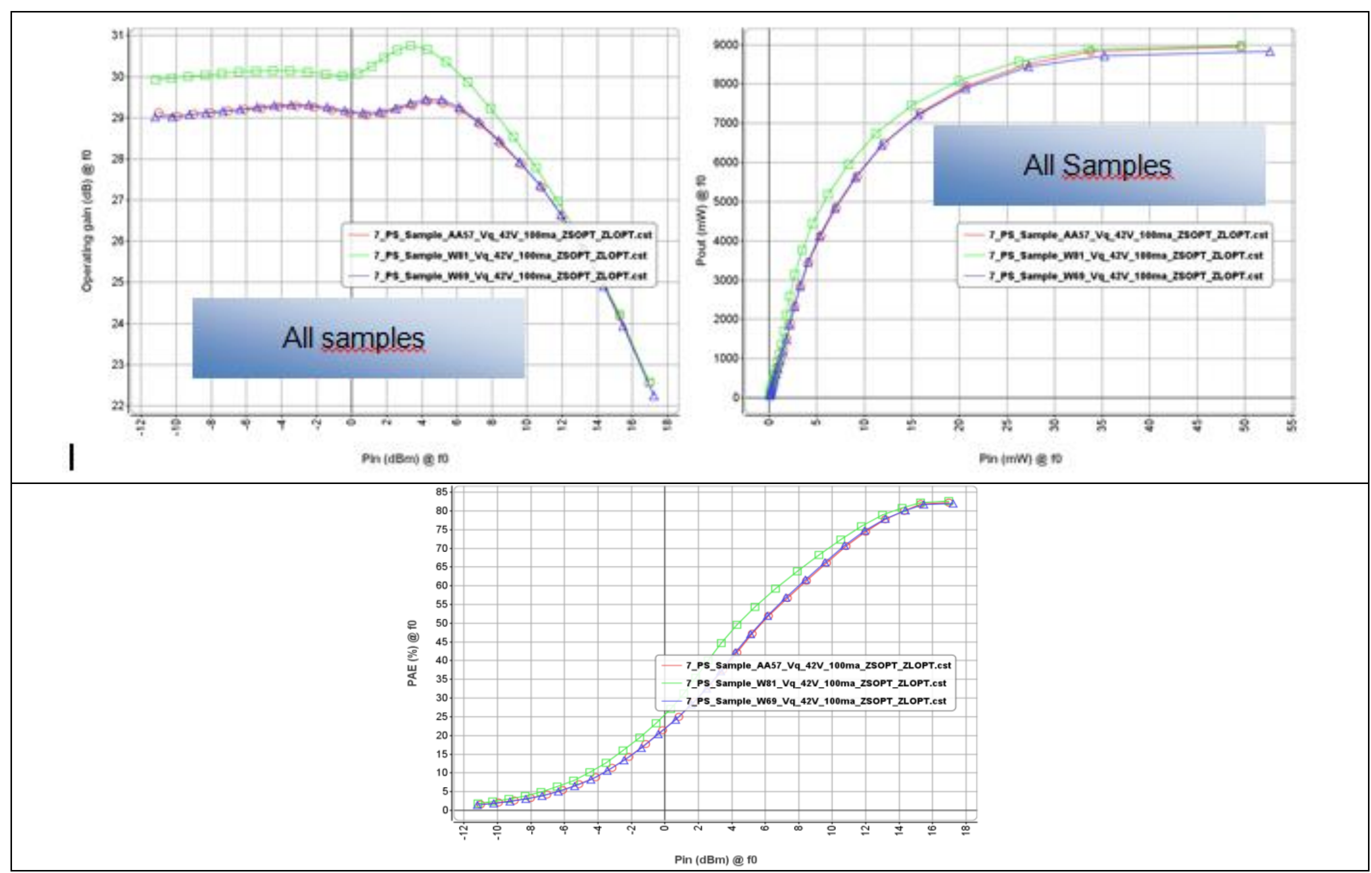

Figure 104 : Loadpull measurements. Performance vs Technology Dispersion. 3x 8x250µm transistor samples tested. 42V, 50mA/mm.

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Table which summarized the load-pull performance monitored during loadpull measurements on different samples is provided below.

Sample	Linear Gain (dB)	Output Power (W)	PAE f0 OPT(%)	PAE all OPT(%)	Zload f0 opt PAE (Ω)	Zload 2f0 opt PAE (Ω)	Zsource f0 (Ω)	Zsource 2f0 (Ω)
W81	29.92	8.97	71.4	82.61	63.27+j83.22	2.08+115.5j	6.17+17.13j	172+266.5j
W69	29.02	8.84	No data	82.02	63.27+j83.22	2.08+115.5j	6.17+17.13j	172+266.5j
AA57	29.12	8.95	No data	82.29	63.27+j83.22	2.08+115.5j	6.17+17.13j	172+266.5j

Table 19 : Summary of performance monitored during loadpull measurements. Vds=42V and Ids=50mA/mm

2.2.3.2 *Unitary cell modeling activity. Run-2*

The provided model is a 3 ports transistor. All the parameters are available as well as the chuck temperature and selfheating effects. The model topology is illustrated below..

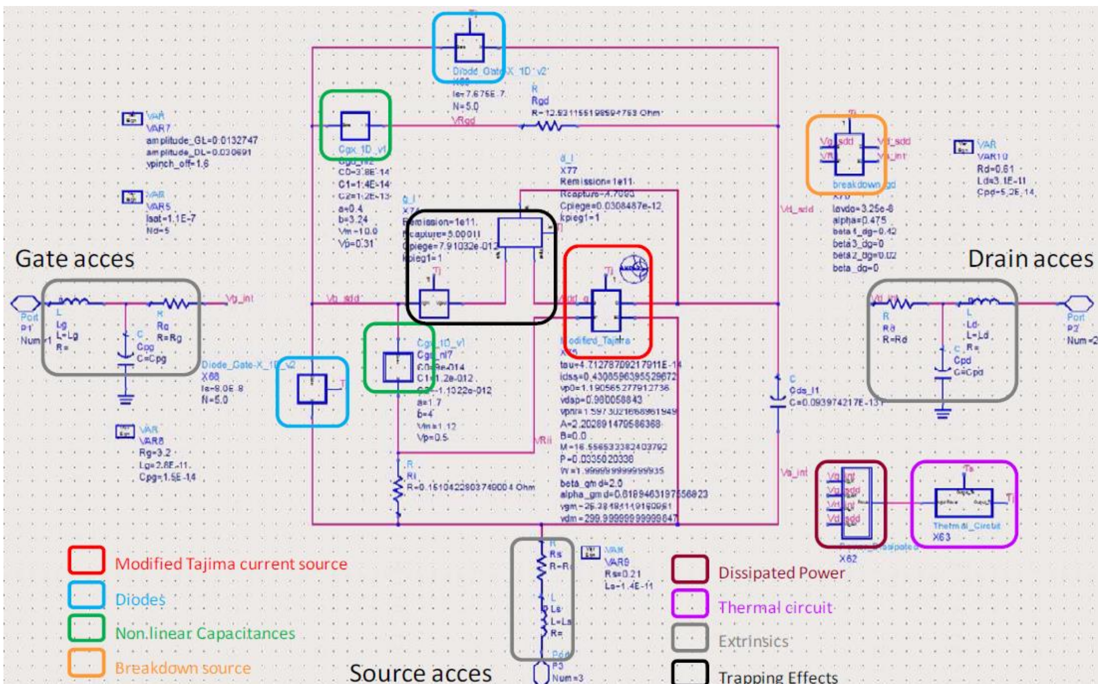

Figure 105 : Elementary transistor cell 8x250µm GH50. Model implemented in ADS

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Input/output access lines: Line_port1 & Line_port2 (Figure II.1) are used for deembedding to consider the transistor plan. All measurements are de-embedded on IVCAD knowing S-Parameters of these input/output access lines inside the transistor plan.
These later were calculated from the provided layout (STARDUST), by THALES ALENIA SPACE. In this chapter, all the comparisons (measurements / model) will be presented in the transistor plan

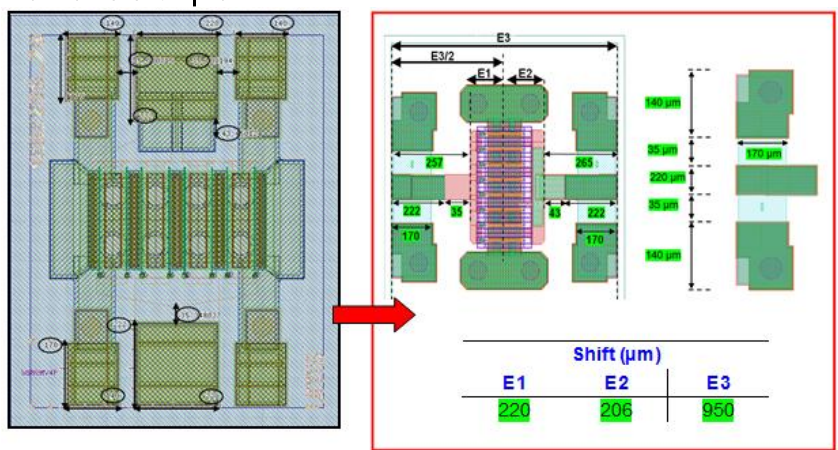

Figure 106 : Access lines & Transistor Layout (All values in µm)

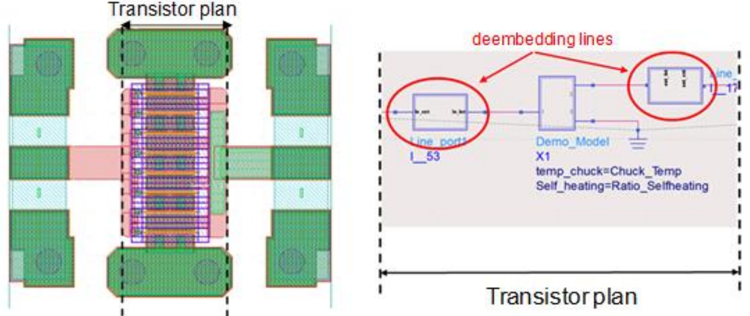

Figure 107 : Modeled Transistor

The model is adjusted through several measurements (I(V), [S], load-pull...) in different operating conditions (bias, temperature, frequency...) in order to have a coherent model. Some comparison (measurements/simulations) are provided below the very good accuracy of the transistor model.

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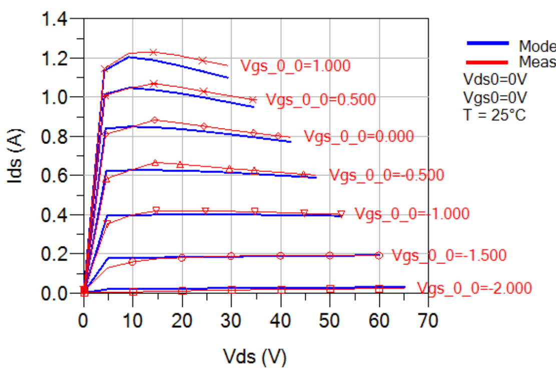


Figure 108 : 8x250µm transistor model validation. I(V) curves comparison. Quiescent bias conditions : Vds0=0V, Vgs0=0V

Thermal network was provided by XLIM through ANSYS. Rth and Cth were then directly implemented on ADS

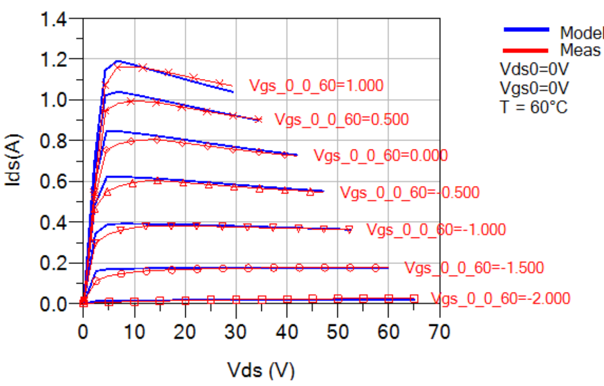
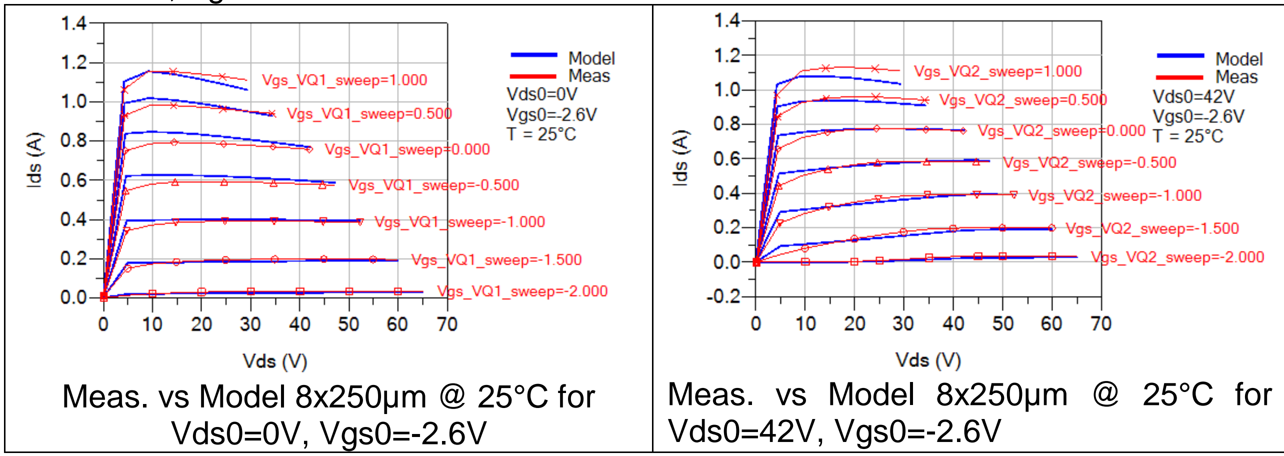


Figure 109 : 8x250µm transistor model validation. I(V) curves comparison. Bias conditions : Vds=0V, Vgs=0V. Temp=60°C

Comparisons between the pulsed I(V) measurements and the model @ _chuck=25°C are illustrated below, for the quiescent bias conditions : Vds0=0V, Vgs0=-2.6V, Vds0=42V, Vgs0=-2.6V.



Meas. vs Model 8x250µm @ 25°C for Vds0=0V, Vgs0=-2.6V	Meas. vs Model 8x250µm @ 25°C for Vds0=42V, Vgs0=-2.6V

Figure 110 : Trap effects

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For S parameters [0.6 to 26 GHz] validation, the model is compared to the measurement on several bias points.

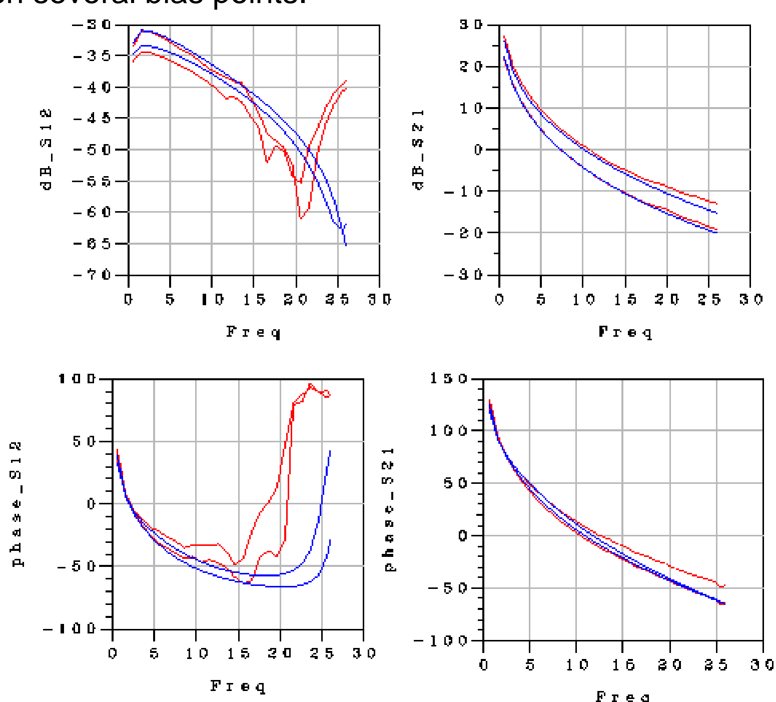

Figure 111 : 8x250µm transistor model validation. [S] parameters comparison. Measurement. vs Model 8x250µm @Vds0=42Vand Ids0=50mA/mm

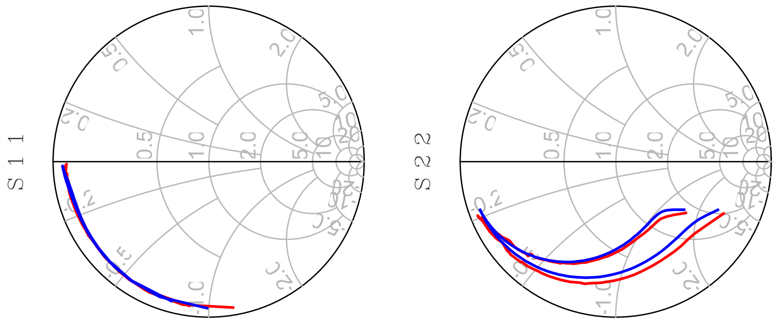

Figure 112 : 8x250µm transistor model validation. [S] parameters comparison. Measurement. vs Model 8x250µm @Vds0=42V and Ids0=50mA/mm

In Load-pull configuration, the comparison is performed at one frequency (1.5385GHz) and for several load impedances including the optimum ones. Next figures illustrate contour of max PAE & opt POUT @ 3dB respectively.

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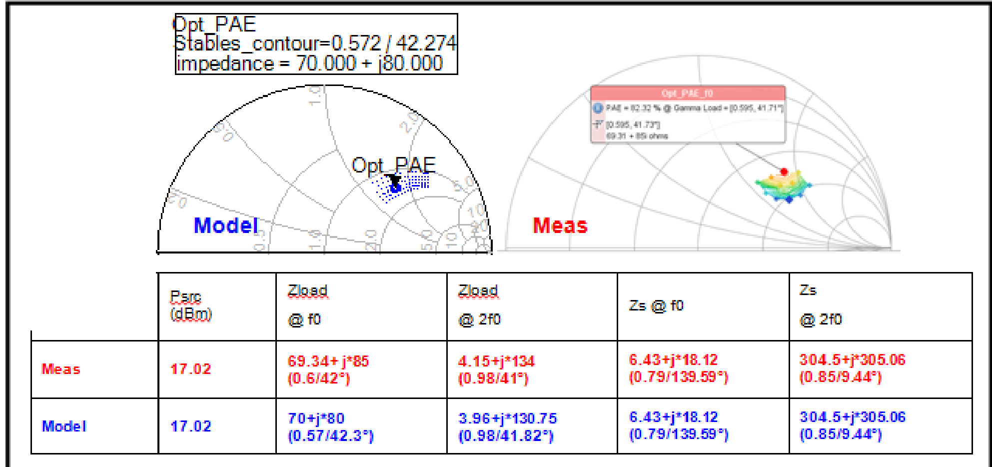
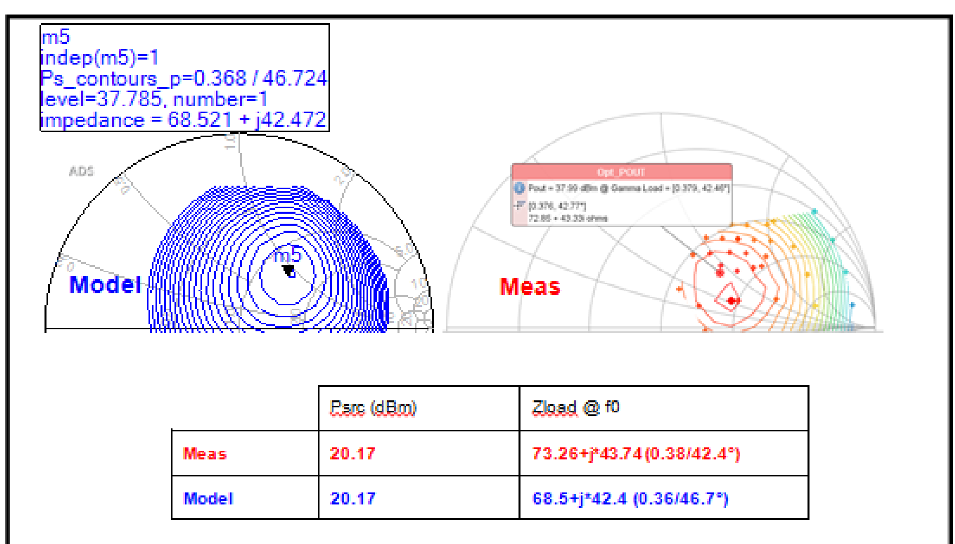


	Psrc (dBm)	Zload @ f0	Zload @ 2f0	Zs @ f0	Zs @ 2f0
Meas	17.02	69.34+j*85 (0.6/42°)	4.15+j*134 (0.98/41°)	6.43+j*18.12 (0.79/139.59°)	304.5+j*305.06 (0.85/9.44°)
Model	17.02	70+j*80 (0.57/42.3°)	3.96+j*130.75 (0.98/41.82°)	6.43+j*18.12 (0.79/139.59°)	304.5+j*305.06 (0.85/9.44°)

Figure 113 : Contour of Max PAE - Meas. vs Model 8x250µm



	Psrc (dBm)	Zload @ f0
Meas	20.17	73.26+j*43.74 (0.38/42.4°)
Model	20.17	68.5+j*42.4 (0.36/46.7°)

Figure 114 : Contour of opt POUT @ 3dB - Meas. vs Model 8x250µm

Opt PAE is reached at very near load impedance on measurements & simulations. On the following table, for comparison (simulation/measurement) exercise, opt PAE & Pout selected at f0, including opt PAE @ 2f0 are presented.

	Zload @ f0	Zload @ 2f0	Zs@ f0	Zs@ 2f0
Opt PAE	**69.34+ j*85 (0.6/42°)**	**4.15+j*134 (0.98/41°)**	**6.43+j*18.12 (0.79/139.59°)**	**304.5+j*305.06 (0.85/9.44°)**
Opt POUT @ 3dB	**73.26+j*43.74 (0.38/42.4°)**			

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Figure 115 : 8x250µm transistor model validation. Loadpull simulations / measurements comparison. Vds0=42Vand Ids0=5OmA/mm

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2.2.3.3 Power Bar measurements. Run-2

Load-pull measurements have been performed by TAS-F at Toulouse facilities. Conditions are:

- 3 power-bar mounted in jig test configuration and tested
- Measurements in CW mode with the following conditions:
- Vds0=42V
- Ids0=800mA (50mA/mm)
- Fc=1.5385GHz
- The measurements have been performed in the SMA connectors plans (before de-embedding)
- De-embedding have been performed by AMCAD during the modeling activities.

The load-pull Optimization methodology used during this campaign is:

- Measurement on Zout_H1=Zout_H2=50ohms
- Measurement on S22*
- Measurement with cloud of points in S22* area
- Measurement with cloud of points at Zout_H1 to obtain PAE_opt
- Measurement with cloud of points at Zout_H2 to obtain PAE_opt
- New optimization of Zload @ F0 with Zload@2F0 optimized
- Final optimization for max PAE: Zload optimum @F0 and 2F0

Final performance after the different loadpull optimization steps are presented below:

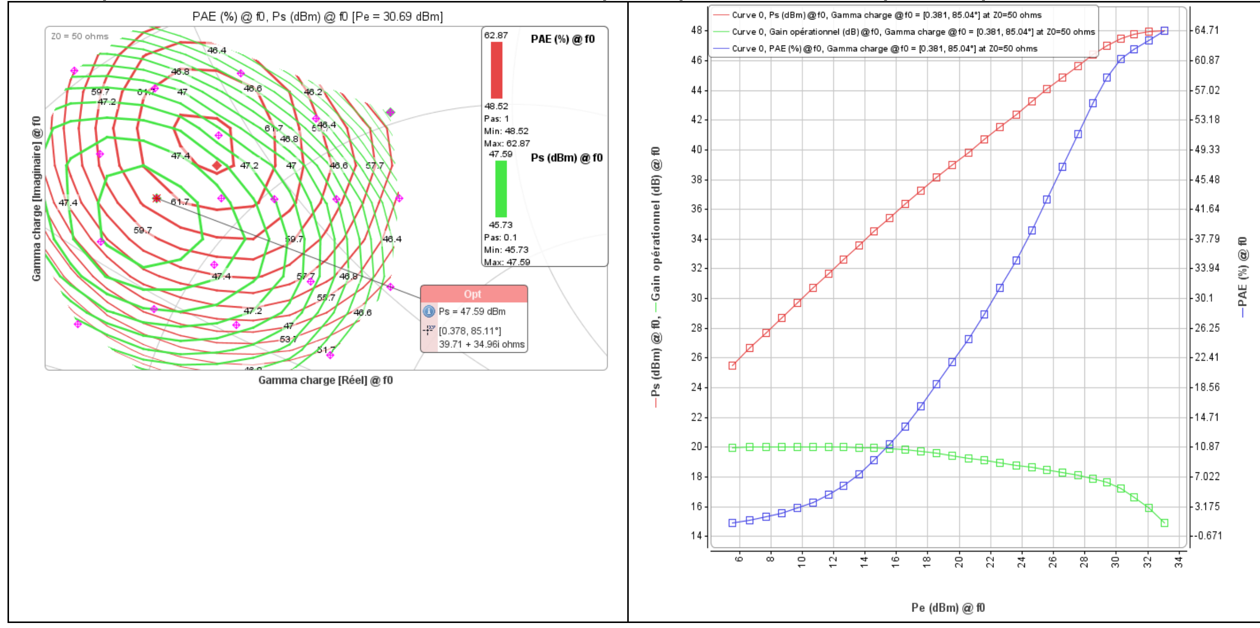

Figure 116 : SMA reference plane, Power bar N°2. Power Gain (dB)/ Pout(dBm) / PAE(%) of the power bar after final optimization of Zload @ F0 and Zload@2F0

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Finally, the measured RF performance of the power bar after final optimization of Zload @ F0 and Zload@2F0 is With this second optimization at fundamental frequency (2F0opt, 3F0 is set to 50 Ohms):

- Ps = 63 W
- PAE = 64,71 %
- Gain = 20 dB
- Zout_H1 : [0,378 ;85,11°]
- Zout_H2 : [0,507 ; 118,2°]

2.2.3.4 *Power Bar modeling activity. Run-2*

The power-bar model includes connections for 8 elementary transistors. Theses later are connected at the drain with a short circuit and through a resistor at the gate. Also, an input resistance “R” is added to describe parasitic effects due to the bonding connection at the input Power-bar. The power bar is connected through wire bondings to input and output circuit. Wires bounding are represented by their S parameters. Input circuit and output circuit are represented either by a simulated circuit or S parameters of these circuits.

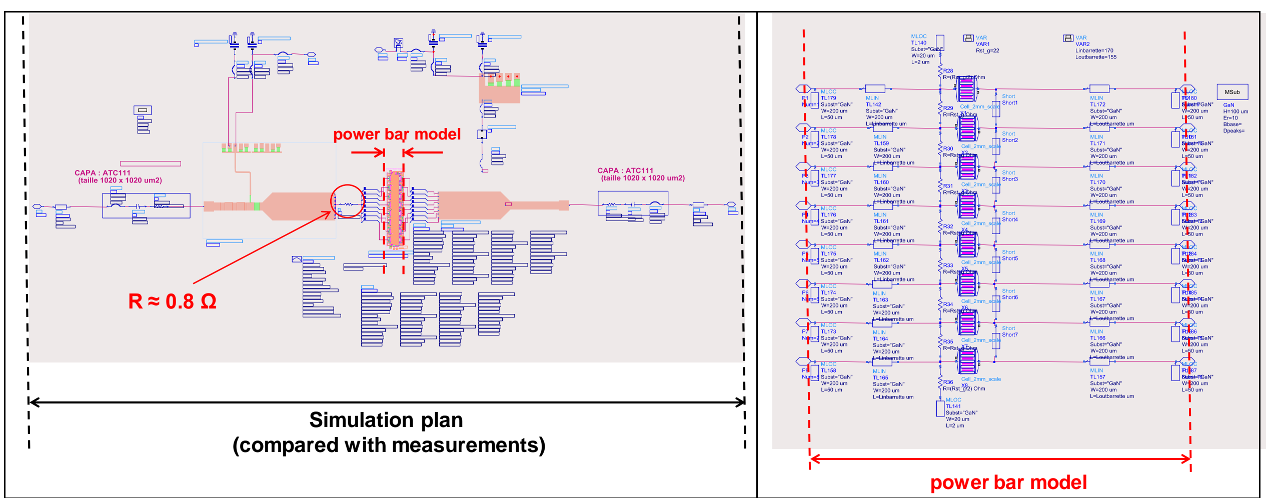
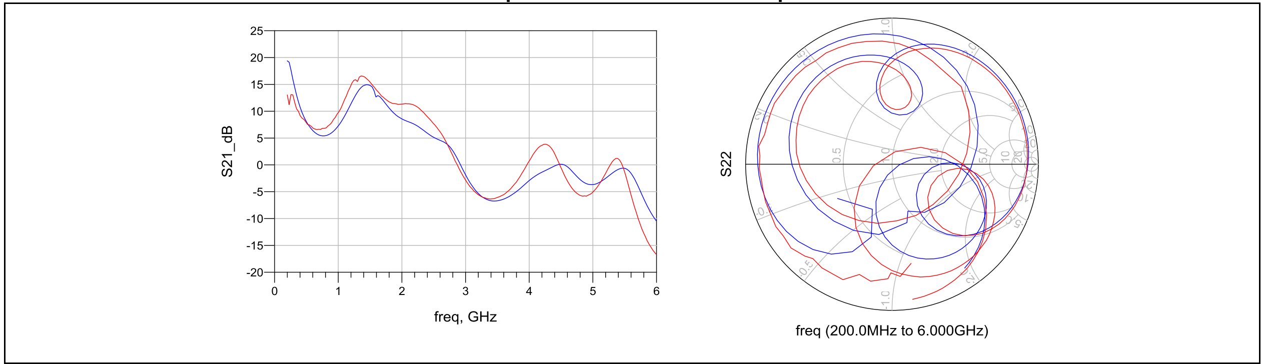


Figure 117 : Used power bar configuration for the simulation

Simulation and measurement comparison results are provided below:



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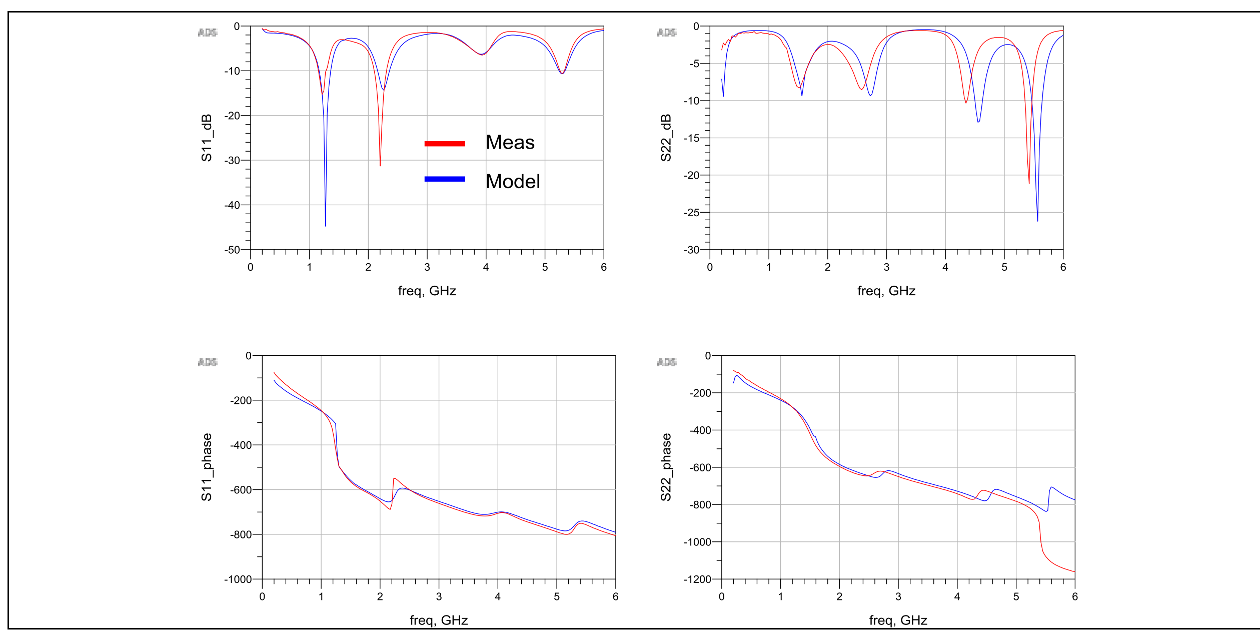

Figure 118 : Sparameter comparison between simulations and measurements for power bar Jig_Test_Barrette_N1

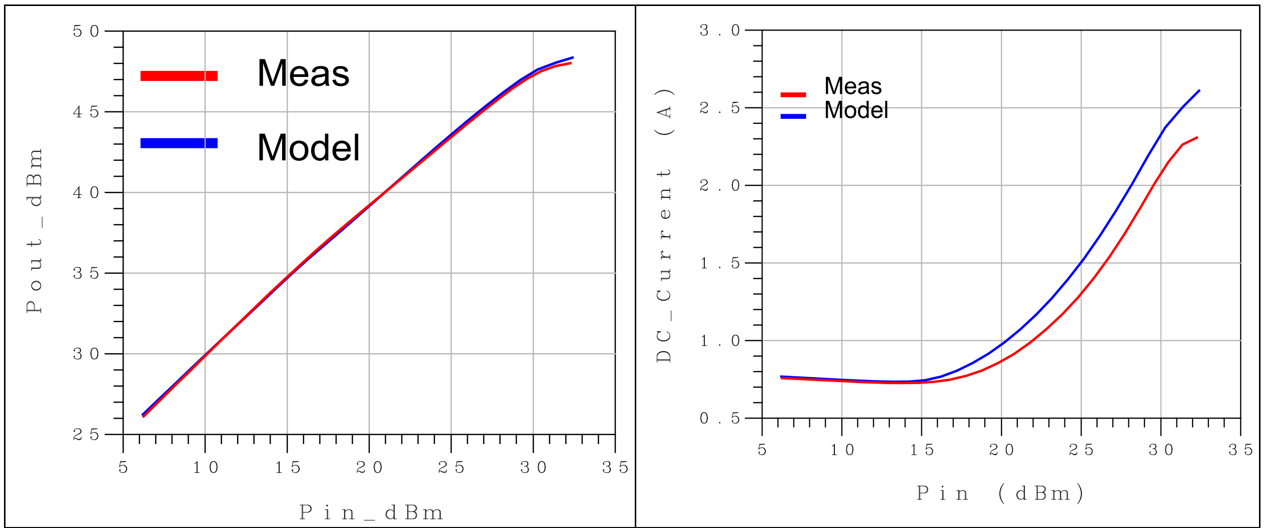

Figure 119 : Pout vs Pin and DC current vs Pin. Comparison between simulation and measurements for power bar N2

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Figure 120 : Input reflexion coefficient / PAE / Gp / AMPM versus Pin. Comparison between simulation and measurements for powerbar N2

2.2.3.5 Synthesis of the performance Gate-Lag and Drain Lag monitored for Sabrina wafer (Run-1) and Stardust wafer (Run-2)

In the frame of this ESA ARTES 5.1 study two wafers have been manufactured:

- GH50 SABRINA wafer manufactured in 2011
- GH50 STARDUST wafer manufactured in 2014

Thus, monitoring of the UMS 0.5 µm GaN process evolution has been performed through the manufacturing of two wafers and associated to the characterizations of transistor cells and power-bars.

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Regarding the evolution of the RF performance of the transistor cells between the two wafers, the following observations have been done:

- Gate Lag on SABRINA, no Gate Lag on STARDUST
- Same Drain Lag on SABRINA and STARDUST
- Kink's effect more important on SABRINA
- Current density high on STARDUST (+8%)

	Ids @ Vgs=+1,25V	% of Gate-lag	% of Drain-lag @ Vds=35V	Estimated Power Max @ Vds=35V on network (0,0)	Estimated Power Max @Vds=35V on network (-3,75, 35V)
Stardust AE50	857mA (714mA/mm)	1 %	16 %	6,3W (5.25W/mm)	5,1W (4,25W/mm)
Stardust AE62	842 (701)	0 %	17 %	6,1 (5,1)	5 (4,15)
Stardust AE74	829 (690)	0 %	22 %	6 (5)	4,7 (3,91)
Sabrina L65	793 (660)	8 %	22 %	5,8 (4,8)	4,1 (3,4)
Sabrina L54	766 (638)	11 %	13 %	5,5 (4,6)	4,2 (3,5)

Table 20 : Monitoring of the UMS 0.5 µm GaN process evolution. Drain-Lag and Gate-Lag

2.2.4 Detailed Design. Run-2

Design of the HPA-1 Run-2 has been undertaken to reach the best possible performances with priority on PAE. first of all, optimal output load impedances at fundamental, second and third harmonic frequency have been searched and identified. Through CCN TAS has modified the center frequency from 1,5675GHz to 1,5385GHz. Indeed, this L-band HPA module is used as power stage of a new L-band GaN SSPA for MSS applications. The useful frequency range shall be [1,518-1,559 GHz] instead of [1,5425-1,5925GHz]. This new equipment will be dedicated to the entire renewal market of constellations of mobile communications satellites.

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	L-Band HPA-1 module				
Performance within Environmental Requirements	**Value**	**Test Conditions**	**C/NC**	**Proposed Value**	**Comments**
Nominal Output power with Multicarrier Signal	>30W	@ 15dB NPR Worst case over temperature	C		
Power Added Efficiency with Multicarrier Signal	>55%	@ 15dB NPR Worst case over temperature	-	>50%	
Centre Frequency	1.5385 GHz	L-band	C		
Bandwidth	>50 MHz	@ Nominal output power	C		
Gain Flatness	+/- 0.25 dB	Over the whole BW for fixed input power	C		
Gain with Multicarrier Signal	> 16 dB	@ Nominal output power	C		
Gain Compression Level with Multicarrier Signal	Max 2dB	@ 15dB NPR Worst case over temperature	-	Max 5dB	@ 15dB NPR Worst case over temperature
Maximum Phase shift	<15 deg	From 30 dB back-off to 4dB compression	-	<30 deg	
Deviation from Linear Phase	2 deg pk-pk	versus frequency within BW	C		
Input Reflexion coefficient	<-10 dB	@ Nominal output power, over BW	C		
2nd harmonic rejection	>30 dBc		C		
Main DC voltage supply	>50V		-	45V	
Temperature	-10deg /+85deg		C		
Pressure	Ambient and 10e-6mbar		C		Multipactor free operation will be demonstrated by calculation with a sufficient margin

Table 21 : HPA-1 module. New required performances for Run-2

Optimum 8x250µm transistor output loads have been determined at both fundamental (H1) and second harmonic (H2) frequency using AMCAD 8x250µm transistor load-pull measurements data.

The results of the load-pull analysis after harmonics optimization is given below:

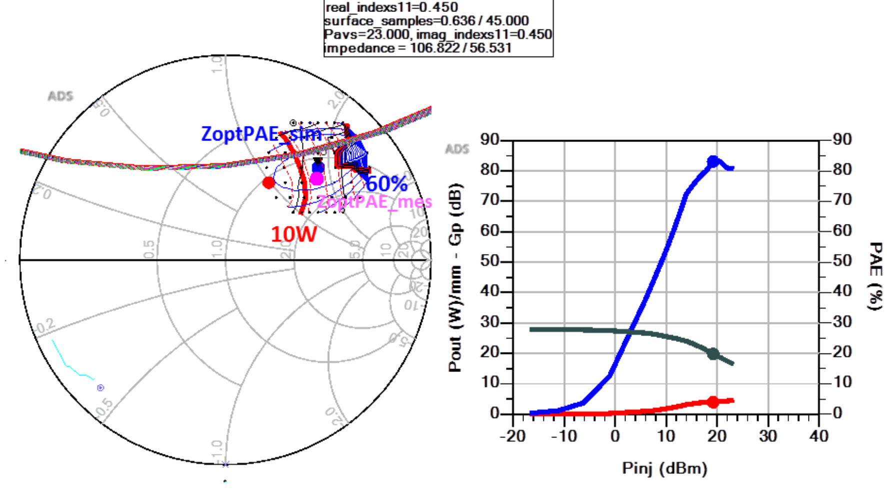

Figure 121 : 8x250µm transistor performance after harmonics loadpull optimization

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Pin (dBm)	Zin (H1)	Zout (H1)	Zout (H2)	Gain lin (dB)	Gain comp (dB)	PAE (%)	Pout (dBm)	Pout (W)	Pout (W/mm)
20	4+j21	58.9+j89	5.5+j110	19.8	8	83	39	7.9	3.95

Table 22 : 8x250µm transistor performance after harmonics loadpull optimization

In order to optimize and predict accurately the HPA performances, package RF insert, capacitors and inductors have been carefully simulated and/or measured to secure the design result. In addition to that, the power-bar has been modeled as precisely as possible by stacking 8 elementary cells in parallel.
The UMS GH50 8x8x250µm power-bar have been made up of 8 elementary transistor stacked together in a way that respect, as much as possible, the power-bar layout provided by UMS. The UMS GH50 8x8x250µm power-bar has been modeled by AMCAD.

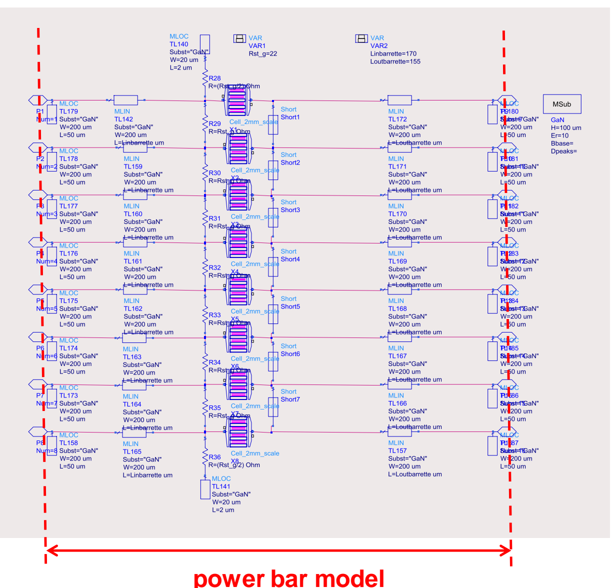

Figure 122 : ADS schematic of the GH50 8x8x250µm powerbar based on AMCAD transistor model

In order to optimize the simulation results, homemade discrete self-inductor model have been used whereas S-parameter files (coming from measurements data) have been used to simulate discrete self-inductors used for DC biasing. Hereafter, you can see the ADS schematic view of the HPA

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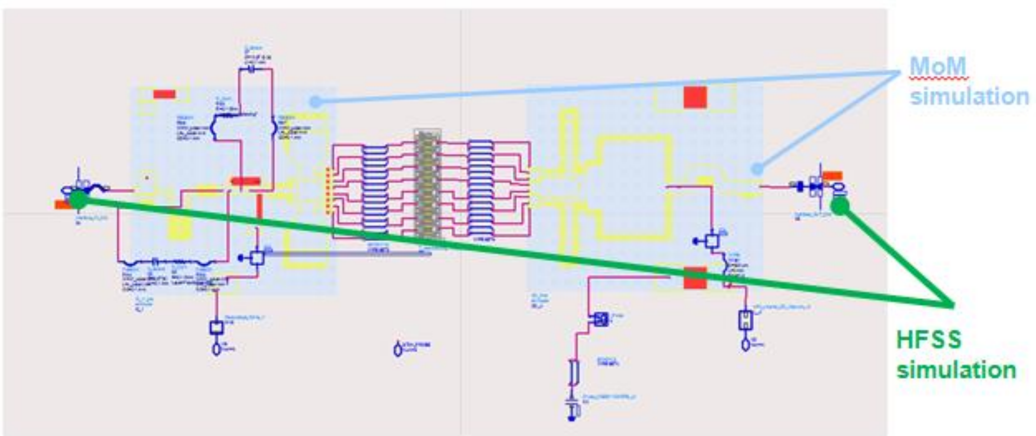

Figure 123 : ADS schematic view of the HPA-1 module Run-2

Due to both input and output matching networks size constraints and the need of high distributed capacitance effect to synthesize appropriate input and output load impedances, high dielectric constant material has been used : Er =40; T=381µm; TanD=0.0003. Input and output combiners have been fully optimized by means of EM simulation up to 10GHz. Engrave resistance sheet (red on Figure 31) has been chosen as low as possible (6Ω/□) to enable the design of resistors in series with the gate of each transistor. In this way, both even and odd mode stability issues have been managed at the same time.
In order to have a more realistic EM simulation result, the all passive components of hybrid HPA are simulated on HFSS, as shown in figure below.

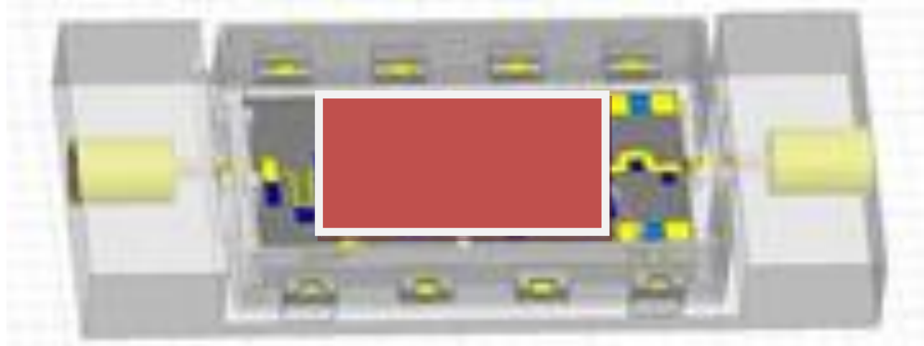

Figure 124 : HFSS schematic view of the HPA-1 module Run-2

The following figures shows the small signal behavior of the HPA in a wide frequency range

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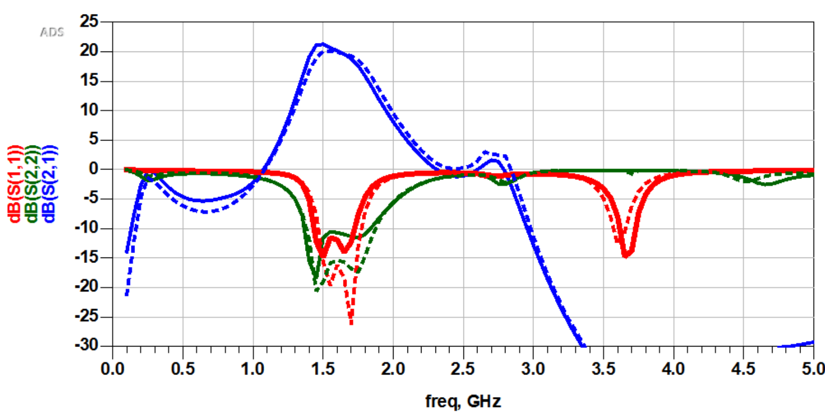

Figure 125 : HPA-1 module. Run-2. Simulated S-parameters wide frequency band analysis

This figure shows that S21 parameter drops below 0dB for frequency higher than 2.2GHz. HPA design have been managed to break the very high gain of the power bar at frequency below 1GHz. In that way, low frequency and Fo/2 oscillation issues will be prevented.

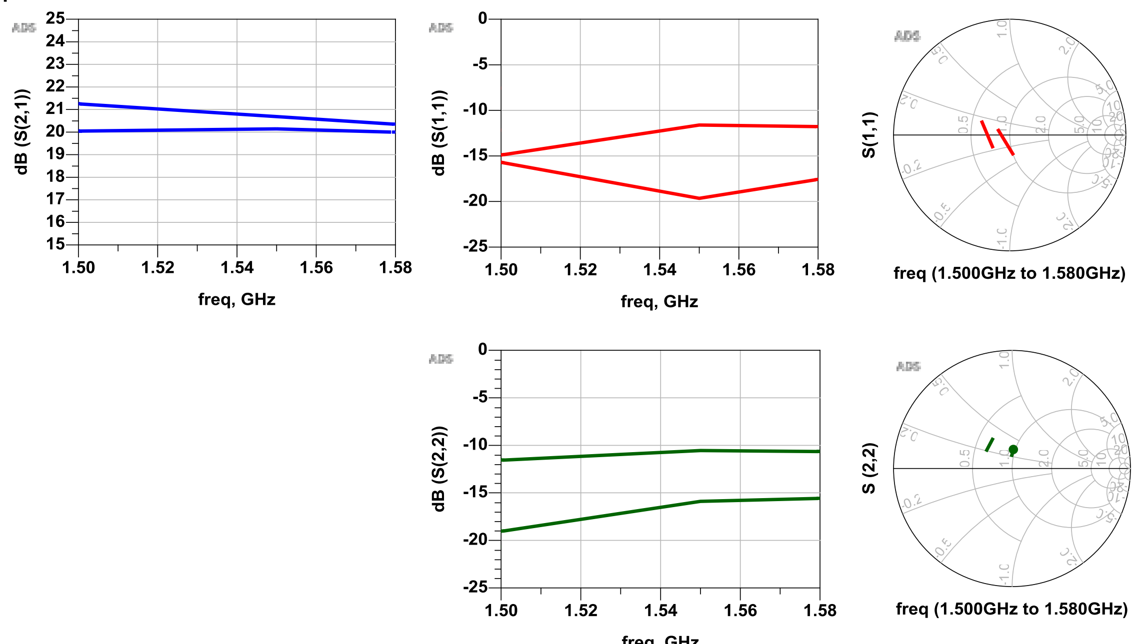

Figure 126 : HPA-1 module. Run-2. Simulated S-parameters in-band frequency analysis

The main RF performances obtained, output power, PAE and power gain are presented below versus input power and versus frequency

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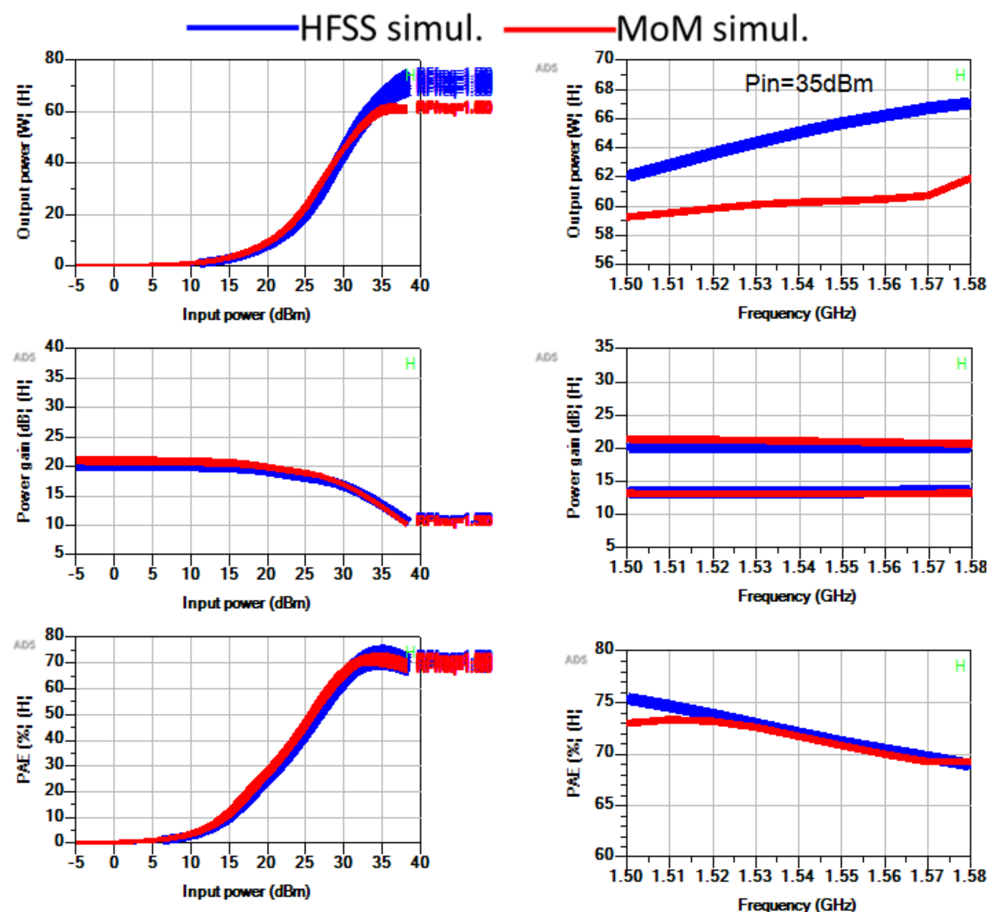

Figure 127 : HPA-1 module. Run-2. Simulated performances. Pout(W), PAE(%), Gain(dB) versus input power (dBm) and Frequency(GHz).

The frequency bandwidth reaches 50MHz for a center frequency of 1.5385 GHz. The maximum overall power added efficiency varies from 69 to 73-75% at Pin = 35dBm and is associated to an output power more than 58W. The maximum PAE value is reached with Pin = 35dBm, which corresponds to a 8 dB of compression. Therefore, the Safe Operating Area is defined as 10 dB of compression. At 35dBm of input power, the mean output power density is around 4 W/mm as shown in figure below.

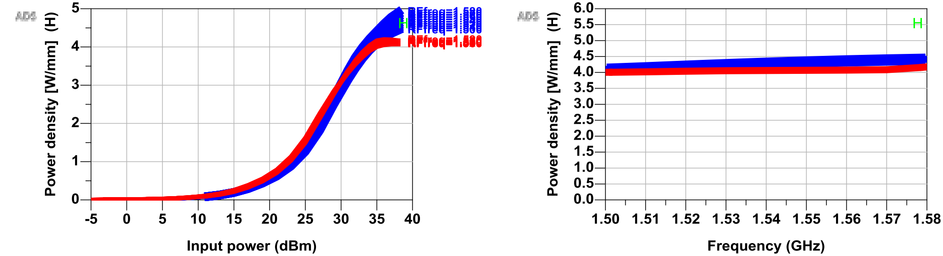

Figure 128 : HPA-1 module. Run-2. Simulated performances. Power density (W/mm) vs. input power(dBm) – from 1.50 to 1.58GHz

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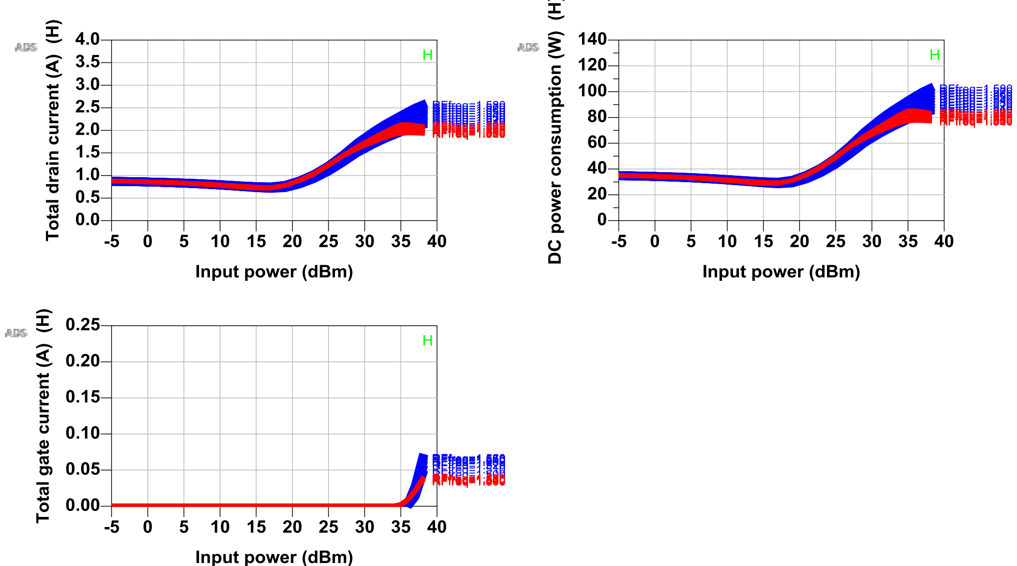

Figure 129 : HPA-1 module. Run-2. Simulated performances. Drain current and power consumption(W) vs. input power(dBm) – from 1.50 to 1.58GHz

Thanks to the electro-thermal capability of the transistor model, the main RF performances; output power, PAE and power gain; of HPA has been checked versus a temperature range from -10°C to 85°C. On figure below, main HPA performances with MoM simulation are shown for an input power (@35dBm) corresponding to the maximum of PAE (Pin = 35dBm)

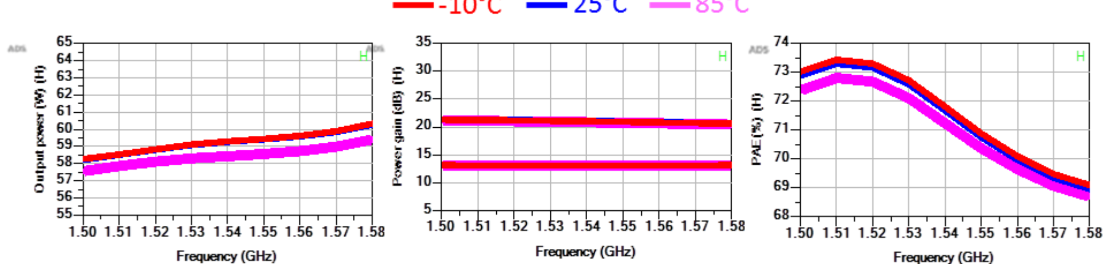

Figure 130 : HPA-1 module. Run-2. Simulated performances : Pout(W), PAE(%), Gain(dB) versus temperature [-10°C; 25°C, 85°C] @Pin(max PAE).

Stability analysis has to be consolidated by STAN software simulations during linear and non-linear operating modes at baseplate temperature equal to -10 °C. . Current probe was placed on transistor gate. For stability analysis is performed using the HPA with MoM simulation.

No critical behavior detected in linear simulation with the following biasing conditions:

- Fixed Ids=50 mA/mm and sweep of Vds from 0V to 45V (step 5V)
- Fixed Vds=40V and sweep of Vgs from -2.2V to -1.2 (step 0.1V)

No critical behavior detected in non-linear simulation at biasing condition (equal to 50mA/mm of drain current and Vds=45V) and with a sweep of input power from -10 dBm to 35 dBm.

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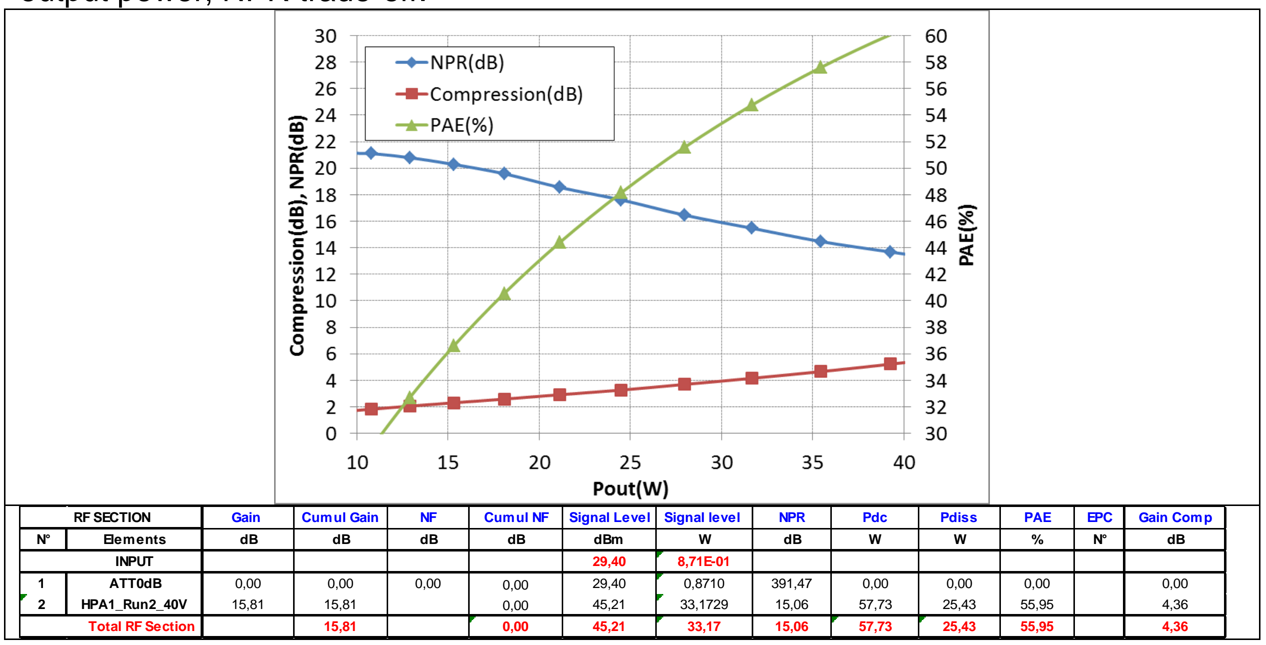
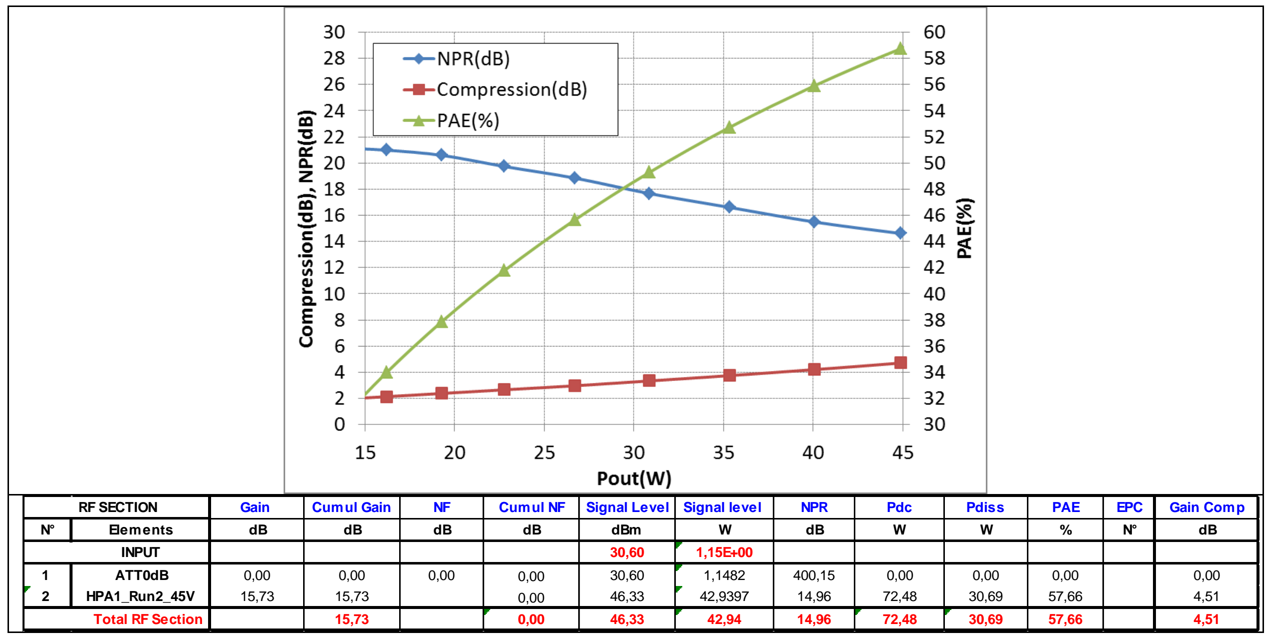
Finally, a Volti analysis has been done at HPA level to check the feasibility of the PAE, output power, NPR trade-off.



RF SECTION		Gain	Cumul Gain	NF	Cumul NF	Signal Level	Signal level	NPR	Pdc	Pdiss	PAE	EPC	Gain Comp
N°	Elements	dB	dB	dB	dB	dBm	W	dB	W	W	%	N°	dB
	INPUT					29,40	8,71E-01						
1	ATT0dB	0,00	0,00	0,00	0,00	29,40	0,8710	391,47	0,00	0,00	0,00		0,00
2	HPA1_Run2_40V	15,81	15,81		0,00	45,21	33,1729	15,06	57,73	25,43	55,95		4,36
	Total RF Section		15,81		0,00	45,21	33,17	15,06	57,73	25,43	55,95		4,36

Figure 131 : HPA-1 module. Run-2. Simulated performances in multi-carrier mode : NPR(dB), compression(dB), PAE(%) versus Pin. Temp=25°C, Vds=40V and Ids=50mA/mm



RF SECTION		Gain	Cumul Gain	NF	Cumul NF	Signal Level	Signal level	NPR	Pdc	Pdiss	PAE	EPC	Gain Comp
N°	Elements	dB	dB	dB	dB	dBm	W	dB	W	W	%	N°	dB
	INPUT					30,60	1,15E+00						
1	ATT0dB	0,00	0,00	0,00	0,00	30,60	1,1482	400,15	0,00	0,00	0,00		0,00
2	HPA1_Run2_45V	15,73	15,73		0,00	46,33	42,9397	14,96	72,48	30,69	57,66		4,51
	Total RF Section		15,73		0,00	46,33	42,94	14,96	72,48	30,69	57,66		4,51

Figure 132 : HPA-1 module. Run-2. Simulated performances in multi-carrier mode : NPR(dB), compression(dB), PAE(%) versus Pin. Temp=25°C, Vds=45V and Ids=50mA/mm

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The tables below summarize the HPA-1 module Run-2 simulated performances reached for the center frequency 1.5385GHz in multi-carriers mode.

Multi-carrier mode : VOLTI analysis Vds=40V and Ids=50mA/mm.	
Parameters	Typ.
Output Power	33,5W
PAE	56%
Gain compression	4,5dB
NPR	15,7dB

Multi-carrier mode : VOLTI analysis Vds=45V and Ids=50mA/mm.	
Parameters	Typ.
Output Power	43W
PAE	57%
Gain compression	4,5dB
NPR	15dB

Table 23 : Summary of simulated multi-carriers performances at HPA-1 module. Run-2. Vd=450V and Vd=45V

2.2.5 HPA-1 Module Manufacturing and Tests. Run-2

3x L-band GaN HPA-1 modules (Sn#01, Sn#02, Sn#03) have been tested: In the frame of this study, tuning of the HPA modules has been performed at Temp=+25°C with CW signal in order to achieve maximum of PAE. Then [S] parameter measurements and power measurements with multi-carrier signal has been conducted.

The results are presented with the following outline

- [S] parameters measurements versus Temp=[-5°C, +25°C, +85°C]
- Power measurements (CW signal) versus Pin. Temp=[-5°C, +25°C, +85°C]. Vds=+40V and RF=[1,5135GHz / 1,5385GHz / 1,5635GHz]
- Power measurements (multi-carrier signal) versus Pin. Temp=[-5°C, +25°C, +85°C]. Vds=+40V, Ids=800mA]
- RF step stress measurements

2.2.5.1 [S] Parameter measurements. Run-2

Hereafter, the Sn#01 module S-parameters are given over a DC to 10GHz bandwidth with drain voltage of +40V and Ids=800mA (50mA/mm) fixed at Temp=+25°C. Measurements are performed versus Temp=[-5°C, +25°C, +85°C]

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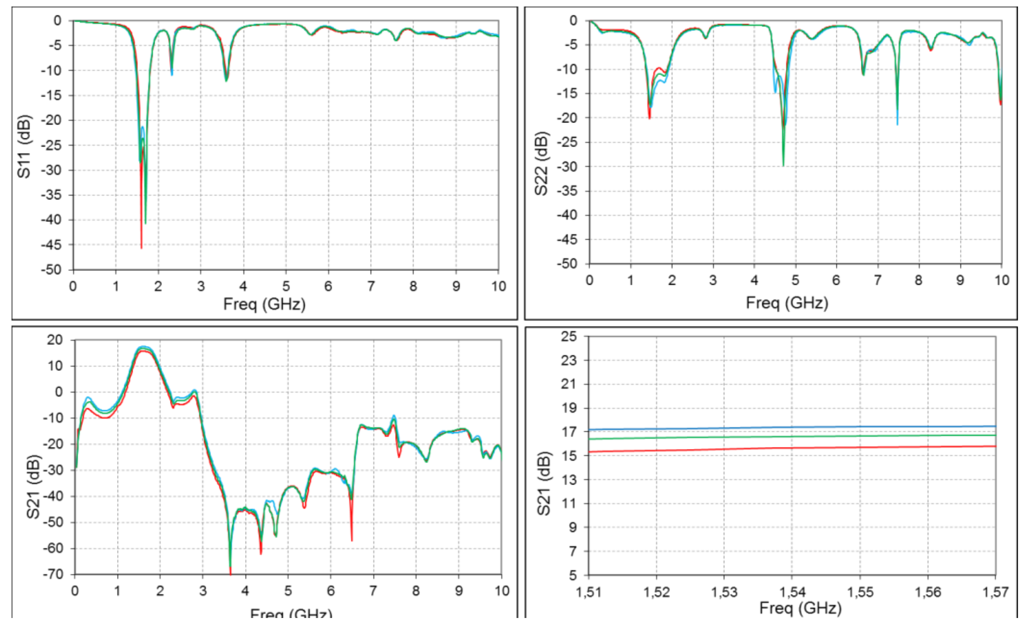

Figure 133 : Run-2. HPA-1 module(Sn#01). [S] parameters measurements. RF=[DC-10GHz], Vd=+40V, Fixed drain current Ids=800mA @+25°C, Temp=[-5°C, +25°C, +85°C]

On the following figures, we focus on the Sn#01 module in-band frequency behavior. Figure shows that S11 and S22 parameters varies not in the same way:

- Input return loss is optimum at hot temperature
- Output return loss is optimum at room temperature.
- S21 variation is about 1,8dB between -5°C to +85°C at 1.5385GHz. At constant gate voltage current, the gain variation versus temperature is 0,2dB/°C

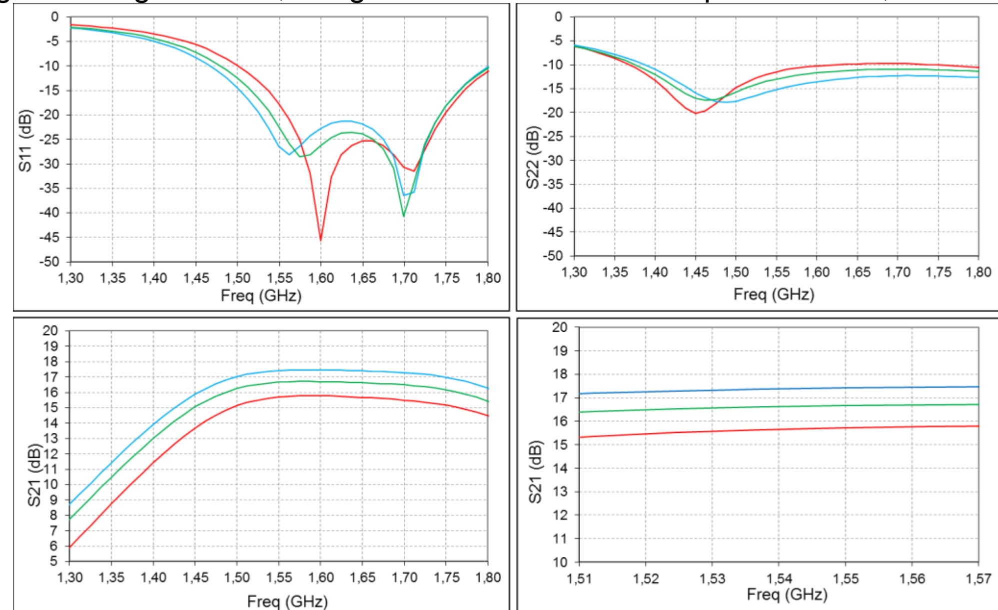

Figure 134 : Sn#01 module. [S] parameters measurements. RF=[1.3-1.8GHz], Vd=+40V, Fixed drain current Ids=800mA @+25°C, Temp=[-5°C, +25°C, +85°C]

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Hereafter, for three HPA modules, the S-parameters are given over a DC to 10GHz bandwidth with drain voltage of +40V and Ids=800mA (50mA/mm) fixed at Temp=+25°C. Measurements are performed versus Temp=[-5°C, +25°C, +85°C]

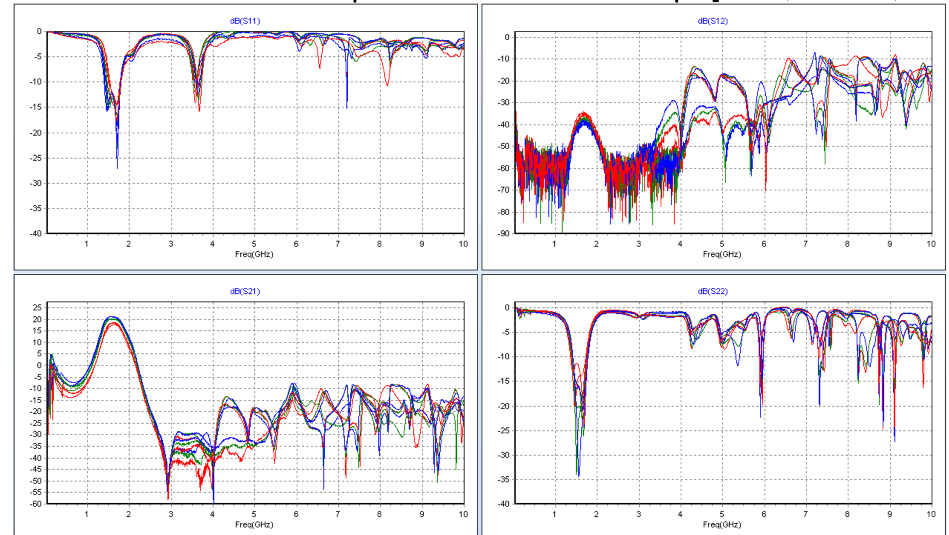

Figure 135 : Run-2. HPA-1 modules. Samples Sn#01 Sn#02 Sn#03 modules. [S] parameters measurements. RF=[DC-10GHz], Vd=+40V. Fixed drain current Ids=800mA @+25°C. Temp=[-5°C, +25°C, +85°C]

On following figures, we focus on the HPA modules in-band frequency behavior. Figure shows the dispersion on S11, S22 and S21 parameters versus HPA modules. Measurements are performed versus Temp=[-5°C, +25°C, +85°C].

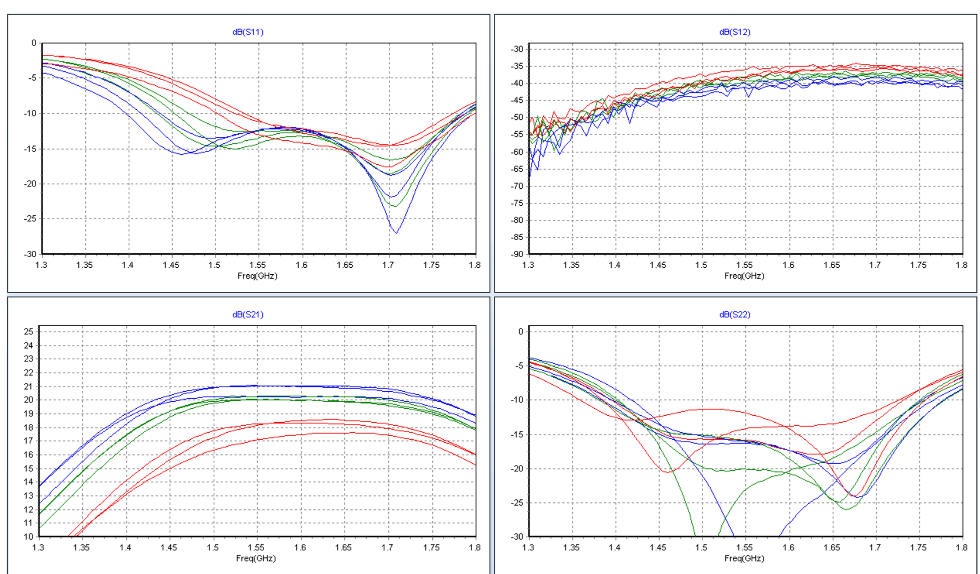

Figure 136 : Run-2. HPA-1 modules. Samples Sn#01 Sn#02 Sn#03 modules. [S] parameters measurements. RF=[1.3-1.8GHz], Vd=+40V. Fixed drain current Ids=800mA @+25°C. Temp=[-5°C, +25°C, +85°C]

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Regarding S21 parameter, at 1,5385GHz, a maximum dispersion of 1dB is observed between the three HPA modules. Regarding S11 parameter, at 1,5385GHz, a maximum dispersion of 2dB is observed between the three HPA modules. Regarding S22 parameter, dispersion is higher compared to the previous parameters. Indeed, depending of the HPA modules, the settings applied on the output combiner to obtain maximum of PAS have an impact of the output return loss behavior.

2.2.5.2 CW mode power measurements. Run-2

The RF performances obtained with a CW signal are presented in this paragraph chapter for Vds=+40V.
The main RF performances obtained, output power, PAE, power gain and phase are presented below versus input power and three frequency points [1,5135GHz, 1,5385GHz, 1,5635GHz]. Measurements have been performed versus Temp=[-5°C, +25°C, +85°C]. For each frequency and each temperature, drain current has been tuned in small signal: Ids=800mA with Vds=+40V.

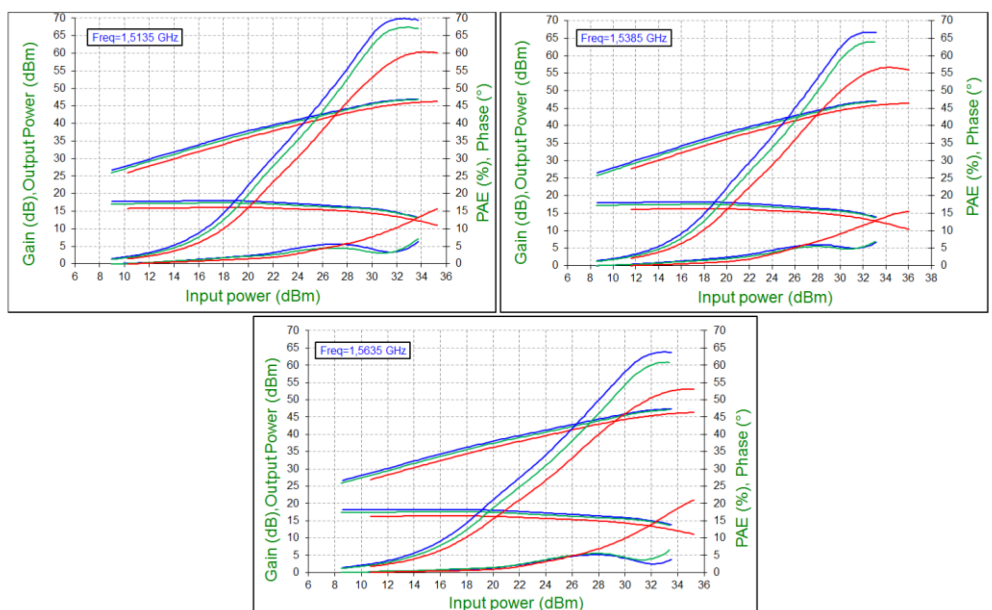

Figure 137 : Run-2. HPA-1 module. Sn#01 sample. Power measurements with CW signal. Temp=[-5°C, +25°C, +85°C], Vd=+40V, Id=800mA. RF=[1,5135GHz / 1,5385GHz / 1,5635GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

The results (Pout, Gain, PAE) are presented versus frequency and temperature. Pin is fixed to obtain maximum of PAE

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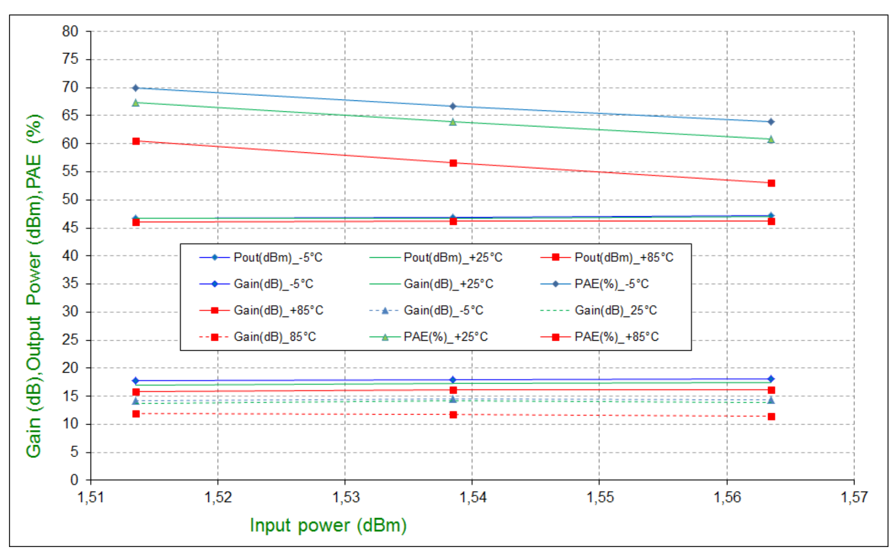

Figure 138 : Run-2. HPA-1 module. Sn#01 module. Power measurements with CW signal. Temp=[-5°C, +25°C, +85°C], Vd=+40V, Id=800mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max.

Synthesis of the RF performances measured with CW signal are provided in the following table

Temp (°C)	Biasing point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	PAE (%)	Phase (°)	Gain (dB)	Compression (dB)
85	Vd=40V,Id=800mA	1,5135	15,77	46,11	40,83	2,55	60,45	13,97	11,94	3,83
		1,5385	16,08	46,18	41,50	2,59	56,64	14,41	11,73	4,35
		1,5635	16,22	46,29	42,56	2,66	53,03	20,32	11,44	4,78
25	Vd=40V,Id=800mA	1,5135	17,04	46,72	46,99	2,94	67,42	5,45	13,69	3,35
		1,5385	17,26	46,74	47,21	2,95	63,92	5,98	14,26	3,00
		1,5635	17,39	47,08	51,05	3,19	60,87	5,98	13,89	3,50
-5	Vd=40V,Id=800mA	1,5135	17,72	46,78	47,64	2,98	69,90	4,03	14,20	3,52
		1,5385	17,94	46,89	48,87	3,05	66,64	5,46	14,56	3,38
		1,5635	18,11	47,26	53,21	3,33	63,89	2,86	14,37	3,74

Figure 139 : Run-2. HPA-1 module. Sn#01. Synthesis of power measurements with CW signal. Temp=[-5°C, +25°C, +85°C], Vd=+40V, Id=800mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

Sn#02 and Sn#03 modules have been tested with the same approach. Synthesis of the RF performances measured with CW signal are provided in the following table

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Temp (°C)	Biasing point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	PAE (%)	Phase (°)	Gain (dB)	Compression (dB)
85	Vd=40V,Id=800mA	1,5135	16,89	46,36	43,25	2,70	64,73	9,83	13,13	3,76
		1,5385	17,05	46,42	43,85	2,74	61,16	10,58	13,32	3,73
		1,5635	17,06	46,82	48,08	3,01	58,15	14,02	12,70	4,36
25	Vd=40V,Id=800mA	1,5135	18,06	46,63	46,03	2,88	69,33	2,16	14,46	3,60
		1,5385	18,21	46,73	47,10	2,94	65,92	3,56	14,66	3,55
		1,5635	18,26	47,07	50,93	3,18	62,93	2,15	14,42	3,84
-5	Vd=40V,Id=800mA	1,5135	18,57	46,68	46,56	2,91	71,62	1,48	14,80	3,77
		1,5385	18,77	46,84	48,31	3,02	68,49	2,34	14,90	3,87
		1,5635	18,87	47,25	53,09	3,32	65,68	0,35	14,62	4,25

Figure 140 : Run-2. HPA-1 module. Sn#02. Synthesis of power measurements with CW signal. Temp=[-5°C, +25°C, +85°C], Vd=+40V, Id=800mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

Temp (°C)	Biasing point	RFfreq (GHz)	Linear Gain (dB)	Pout (dBm)	Pout (W)	Power Density (W/mm)	PAE (%)	Phase (°)	Gain (dB)	Compression (dB)
85	Vd=40V,Id=800mA	1,5135	15,87	46,59	45,60	2,85	63,89	10,90	12,66	3,21
		1,5385	15,67	46,77	47,53	2,97	60,65	15,76	12,32	3,35
		1,5635	15,24	47,06	50,82	3,18	57,61	16,90	12,03	3,21
25	Vd=40V,Id=800mA	1,5135	17,28	47,07	50,93	3,18	69,71	1,09	14,08	3,20
		1,5385	17,08	47,22	52,72	3,30	66,26	1,12	13,83	3,25
		1,5635	16,65	47,57	57,15	3,57	62,86	0,64	12,98	3,67
-5	Vd=40V,Id=800mA	1,5135	17,73	47,13	51,64	3,23	71,97	0,31	14,72	3,01
		1,5385	17,52	47,38	54,70	3,42	68,66	-1,44	13,96	3,56
		1,5635	17,09	47,69	58,75	3,67	65,28	-4,38	13,17	3,92

Figure 141 : Run-2. HPA-1 module. Sn#03. Synthesis of power measurements with CW signal. Temp=[-5°C, +25°C, +85°C], Vd=+40V, Id=800mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

2.2.5.3 Multi-carrier mode power measurements. Run-2

In the following part, multicarrier measurements are presented for two HPA modules: SN#02 and Sn#04. HPA modules have been tested with Vds=40V and biasing point fixed in small signal Ids=800mA. Multi-carrier measurements have been performed at Temp=[-20°C, 25°C, 85°C].

Characteristics of the multicarrier signal applied:

- Centre Frequency: Fc=1.5385GHz
- Bandwidth: Span=50MHz
- Number of carriers: 3000
- Notch: 1%
- Position of the notch: centered at 1.5385GHz

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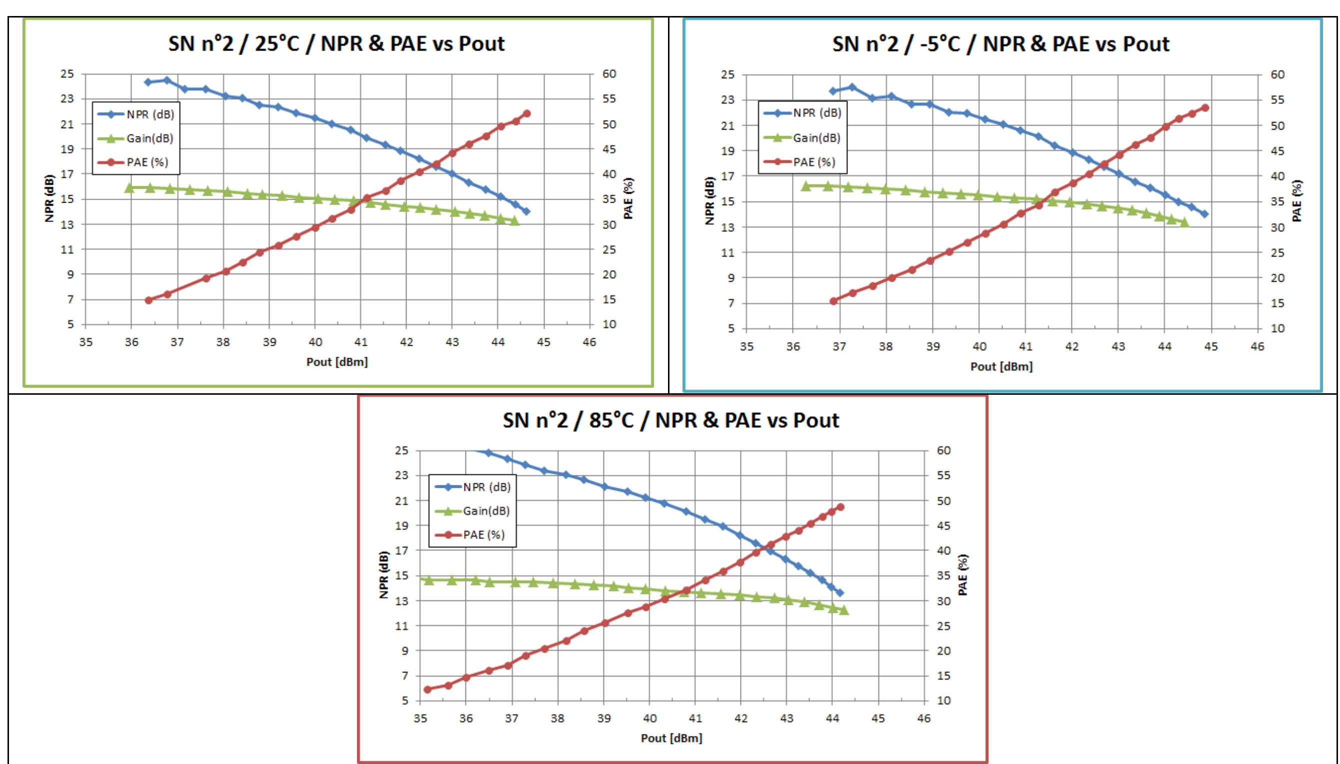

Figure 142 : Run-2. HPA-1 module. Sn#02 Power measurements with multi-carrier signal. Temp=[-5°C, +25°C, +85°C]. Vds=40V, RF=1,5385GHz, Gain(dB), PAE(%), NPR(dB) vs Pout(dBm)

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	Power Density (W/mm)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=40V, Id=800mA, Temp=25°C	15,9	30,3	43,9	24,5	1,5	50,1	14,9	13,6	2,3
		31,1	44,4	27,2	1,7	52,1	14,1	13,3	2,6

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	Power Density (W/mm)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=800mA, Temp=-10°C	16,3	30,0	43,9	24,5	1,5	51,4	15,0	13,9	2,4
		31,1	44,4	27,7	1,7	53,6	14,0	13,4	2,9

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	Power Density (W/mm)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=900mA, Temp=85°C	14,8	30,0	44,0	25,0	1,6	46,2	14,9	12,8	2,0
		31,8	44,1	25,9	1,6	48,4	13,9	12,4	2,5

Figure 143 : Run-2. HPA-1 module. Sn#02 module. Synthesis of power measurements with multi-carrier signal. Temp=[-20°C, +25°C, +90°C]. Vds=40V,

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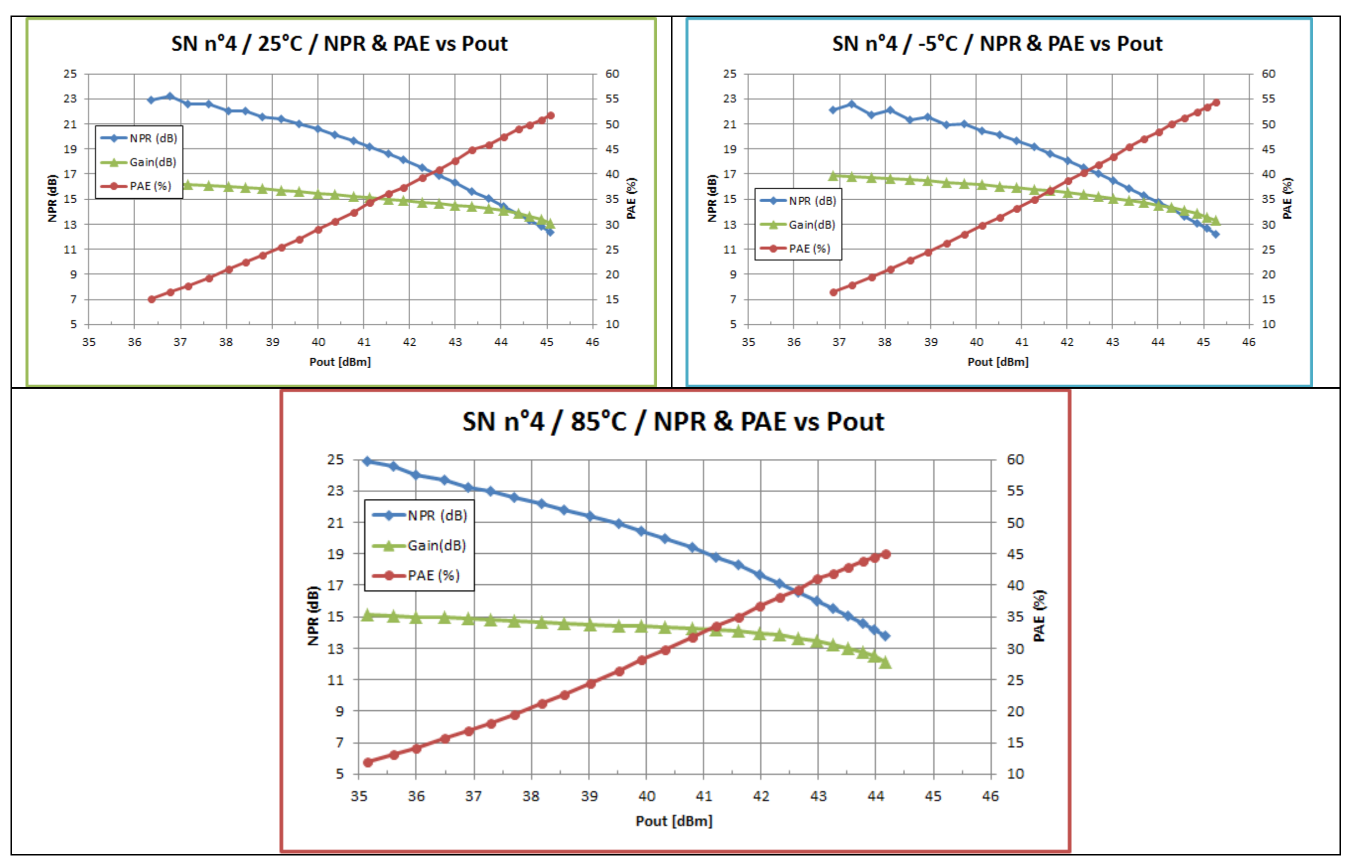

Figure 144 : Run-2. HPA-1 module. Sn#04 Power measurements with multi-carrier signal. Temp=[-5°C, +25°C, +85°C]. Vds=40V, RF=1,5385GHz, Gain(dB), PAE(%), NPR(dB) vs Pout(dBm)

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	Power Density (W/mm)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=40V, Id=800mA, Temp=25°C	16,3	29,5	43,7	23,6	1,5	45,8	15,0	14,2	2,1
		30,3	44,2	26,4	1,7	48,2	14,1	14,0	2,3

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	Power Density (W/mm)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=800mA, Temp=-10°C	16,8	29,2	43,9	24,3	1,5	47,7	15,0	14,6	2,2
		30,2	44,4	27,8	1,7	52,9	13,9	14,2	2,6

	Linear Gain(dB)	Pin(dBm)	Pout (dBm)	Pout(W)	Power Density (W/mm)	PAE (%)	NPR (dB)	Gain (dB)	Compression (dB)
Vd=45V, Id=900mA, Temp=85°C	15,1	30,5	43,5	22,5	1,4	42,9	15,0	13,0	2,1
		31,7	44,1	25,5	1,6	44,7	14,0	12,3	2,8

Figure 145 : : Run-2. HPA-1 module. Sn#04 module. Synthesis of power measurements with multi-carrier signal. Temp=[-20°C, +25°C, +90°C]. Vds=40V,

2.2.5.4 RF step measurements with multi-carrier signal : reliability of GH50-10 technology. Run-2

This paragraph summarizes the reliability test performed on GaN HPA L Band in the frame of the ARTES 5.1 ''SSPAs with European GaN Devices'' study. The goal of this reliability study is to define a Safe Operating Area through RF Multicarrier step stress

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(1 dB compression, 3 dB compression, 5 dB compression). For that, a dedicated multicarrier test bench have been developed. Intermediate RF measurements and in situ monitoring are performed during this qualification.
Test plan is provided in the following table:

	Function	HPA 50 WATTS 16 mm
	Process	UMS GH50-10
	Frequency	1.56 GHz
	DC Bias	Vd=45V, Id = 100 mA (6,25 mA / mm)2 samples + 1 sample Id=400 mA (25 mA / mm)
DC Life test	Number of Sample	NA
	T° JUNCTION (Objective)	NA
	Electrical constraint	NA
	Duration	NA
RF Life test	Number of Sample	3 + 1
	T°	25°C
	DC Biases	Nominal DC biases
	Electrical Constraint	Multicarrier
		1 - Step stress :
		2 weeks / step from 4 dBc to 8 dBc
		2 - RF Life test :
		2000 hours @ XdBc - 2 dB or max PAE
	Monitoring	Gate, drain current, Input, output power
	Initial, Final & Intermediate Measurement	RF Characteristic : Pout, Gain, Id, Ig vs Pin, Phase vs input power

Table 24 : Test plan for RF step stress measurements of L-band GH50 HPA-1 module

4 samples have been tested during RF step stress with multicarrier signal:

- Sample n°2 = SN2
- Sample n°3 = SN3(control sample reference)
- Sample n°4 = SN4
- Sample n°5 = SN5

Multi carrier signal is generated using white noise source. The « white noise » bandwidth is = 28 MHz. All the spike > 40 dBc outside the signal band width are eliminated. Synoptic and photographs of the multi-carrier test bench are provided in the following figures.

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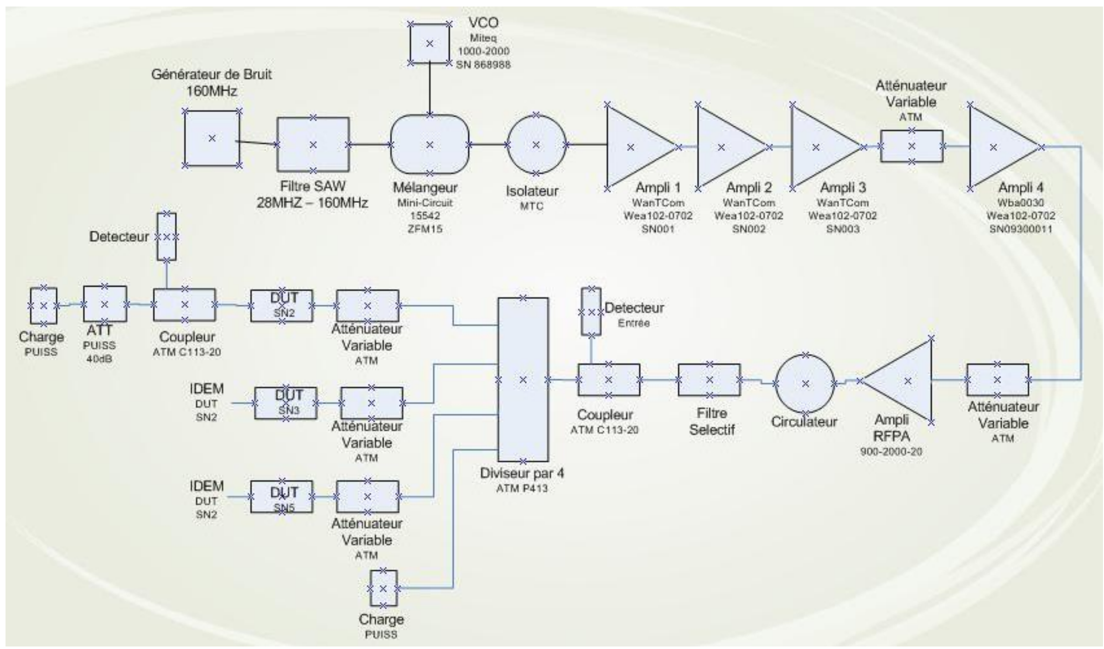

Figure 146 : Multi-carrier test bench

A dedicated test bench for initial, intermediate and final measurement bench is used for [S], AM/AM and AM/PM measurements after each step of compression (2 weeks / step from 1dBc to 5dBc). Synoptic and photographs of this test bench are provided in the following figures.

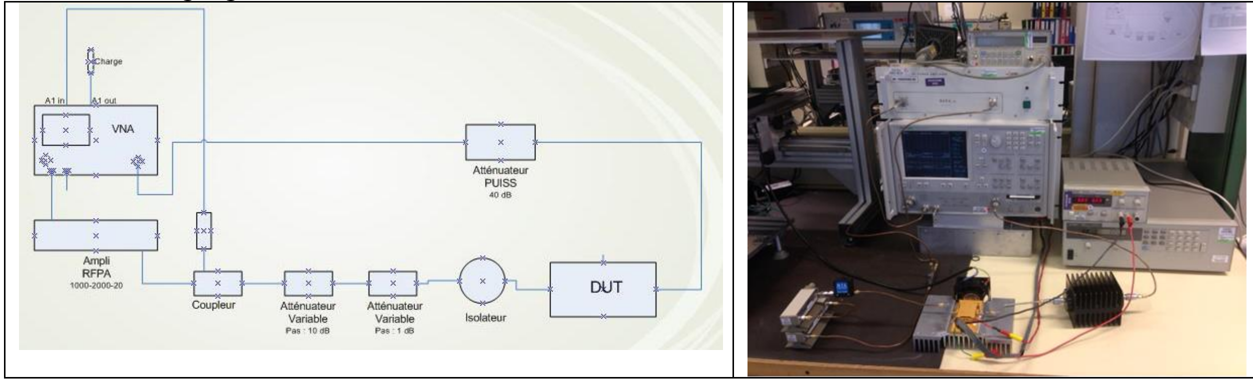

Figure 147 : Photography of the CW test bench for CW initial/intermediate and final measurements

In order to determine the power value during the in situ monitoring we use a detector. The power value versus the detected voltage is represented in the following graph.

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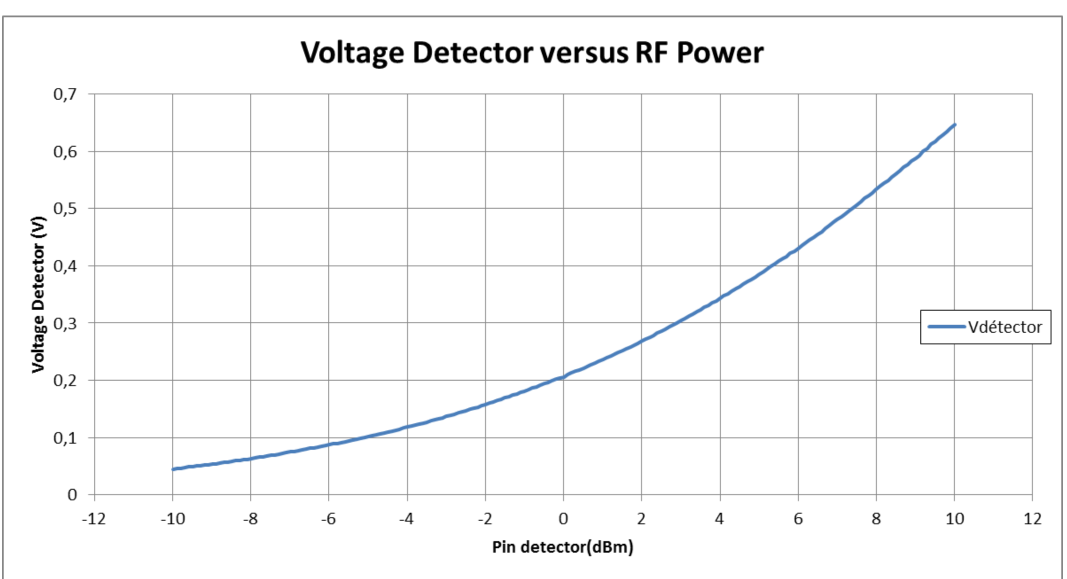
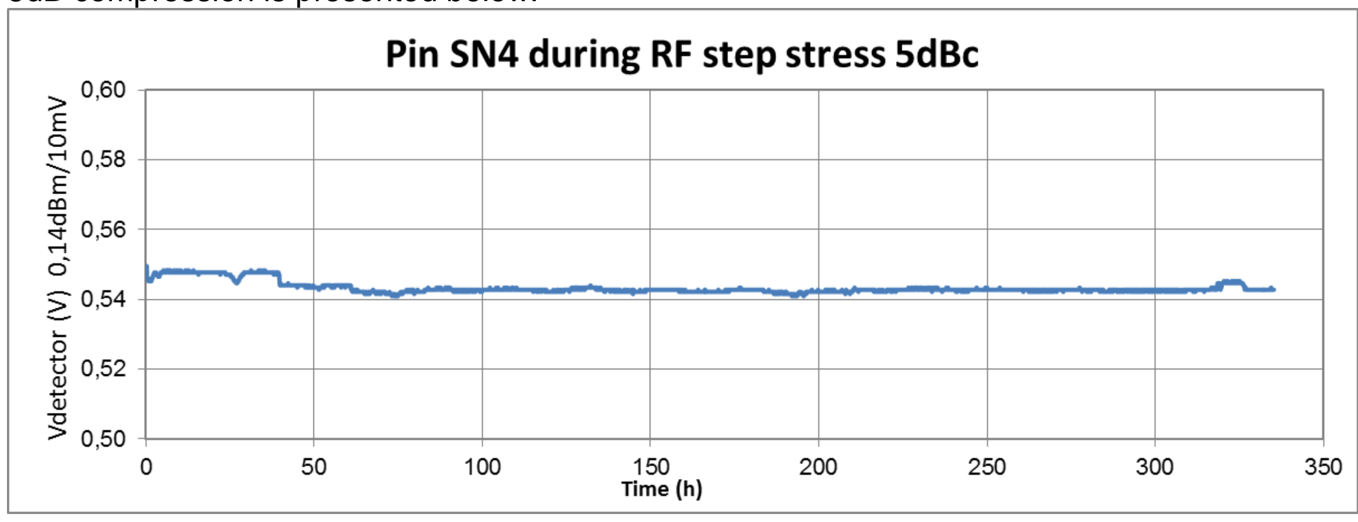


Figure 148 : Detector characterization : Detected voltage value (mV) versus power range(dBm)

On three HPA-1 (Run-2) modules (#2, #4, #5), in Situ measurements have been continuously performed during steps @1dB, @3dB, @5dB. The different parameters monitored are:

- Input power (dBm) and output power (dBm)
- Temperature (°C)
- Drain voltage (V) and Drain current (mA)
- Gate voltage (V) and gate current (mA)

An example of the in situ monitoring performed on HPA-1 (Run-2) module (#4) at Step 5dB compression is presented below:



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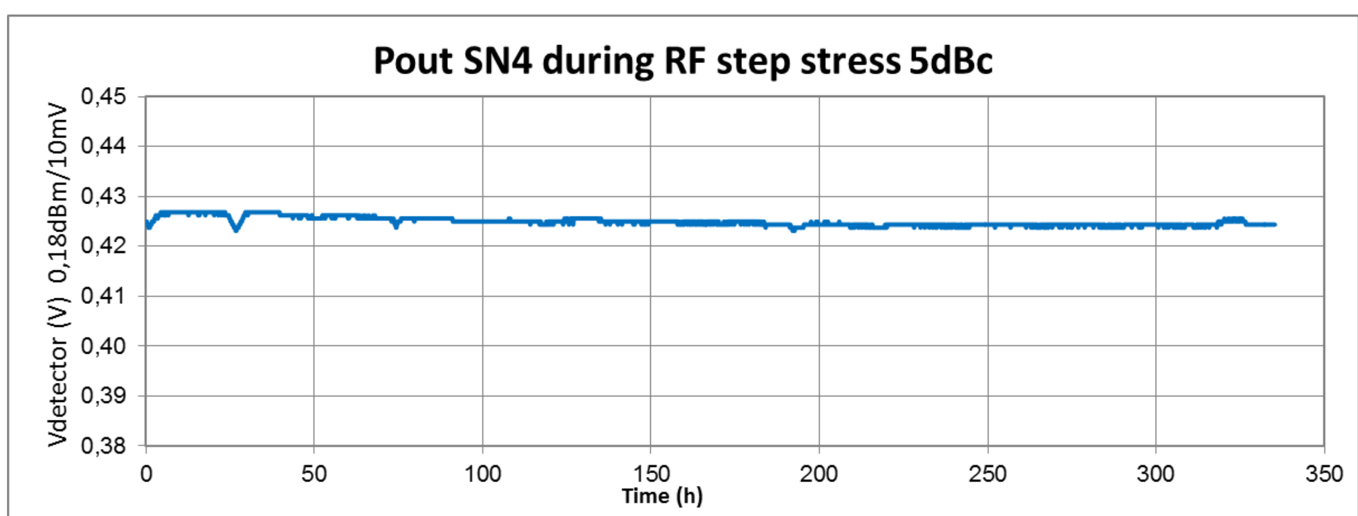

Figure 149 : HPA-1 module Run-2 (#4). RF step stress measurement. Input power and output power monitoring during 5dBc compression step

Vd SN4 during RF step stress 5dBc
Vd (V)
45
40
35
30
25
20
15
10
5
0
0
50
100
150
200
250
300
350
Time (h)

Id SN4 during RF step stress 5dBc
Id (A)
2,10
2,05
2,00
1,95
1,90
1,85
1,80
0
50
100
150
200
250
300
350
Time (h)

Figure 150 : HPA-1 Run-2 module (#4). RF step stress measurement (5dBc step). Drain voltage drift(V). Drain current drift (mA).

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Vg SN4 during RF step stress 4dBc

Ig SN4 during RF step stress 4dBc

Figure 151 : HPA-1 Run-2 module (#4). RF step stress measurement (5dBc step). Gate voltage drift (V) & Gate current drift (mA).

For each HPA-1 module (#2, #4, #5), initial, intermediate and final have been performed. These measurements have consisted of:

- [S] parameters measurements
- CW characterizations (AMAM and AMPM)
- Static measurements

Measurement data are presented for HPA-1 Run-2 module #4 in the following graphs. For the following graphs, the legend is:

- Et0 -> Initial measurements
- Et1 -> Measurements after step @ 1 dBc
- Et2 -> Measurements after step @ 3 dBc
- Et3 -> Measurements after step @ 5 dBc

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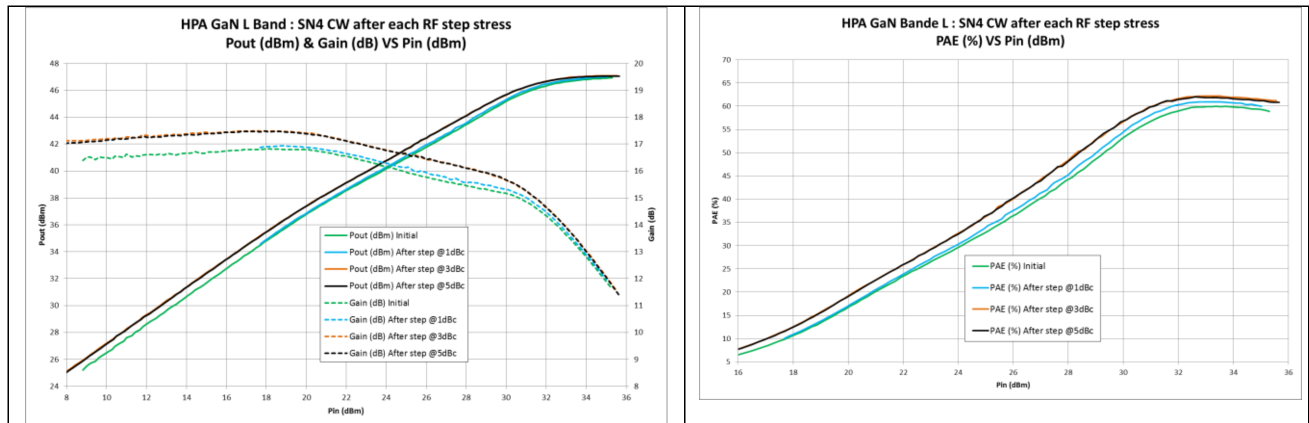
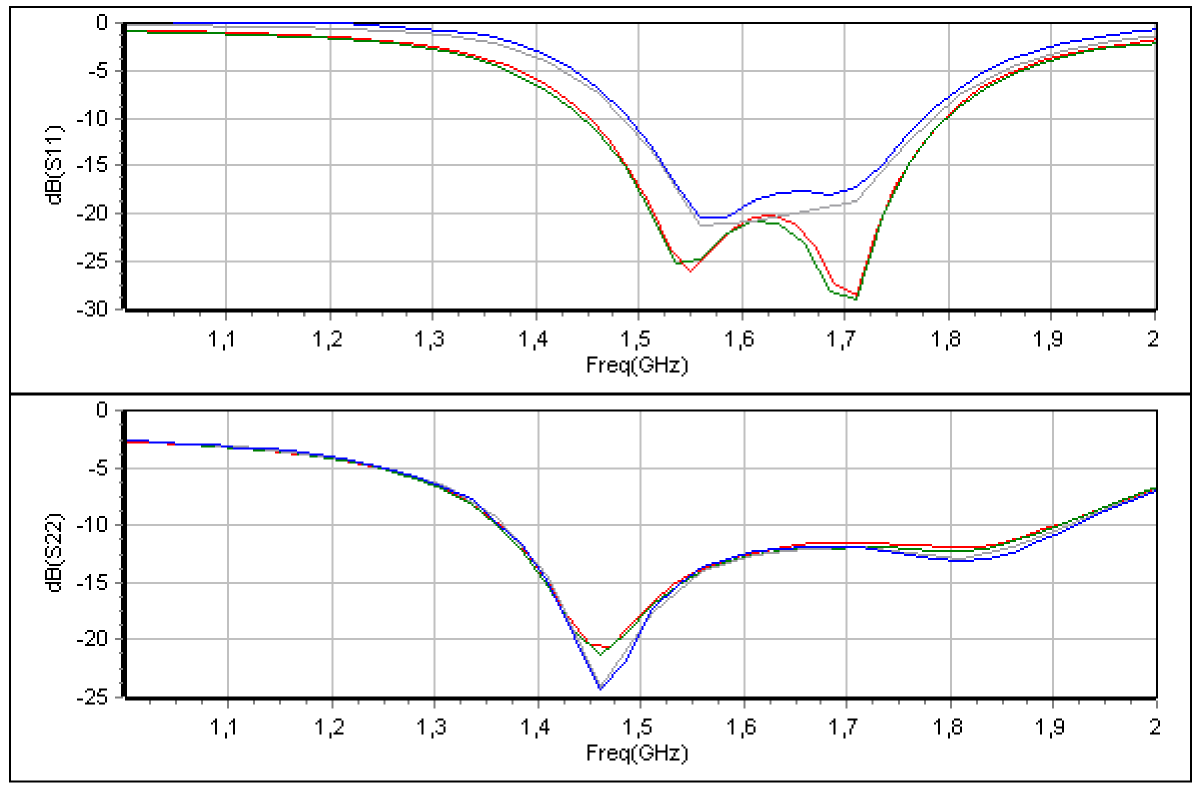


Figure 152 : HPA-1 Run-2 module #4. AMAM and AMPM characterization in CW mode after each compression step of the RF step stress measurements



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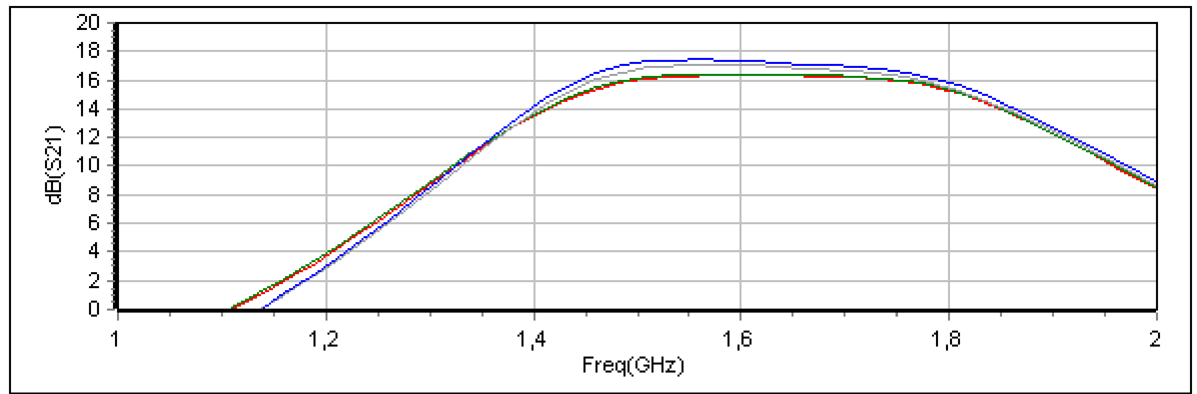

Figure 153 : HPA-1 Run-2 module #4. [S] parameters measurements after each compression step of the RF step stress measurements

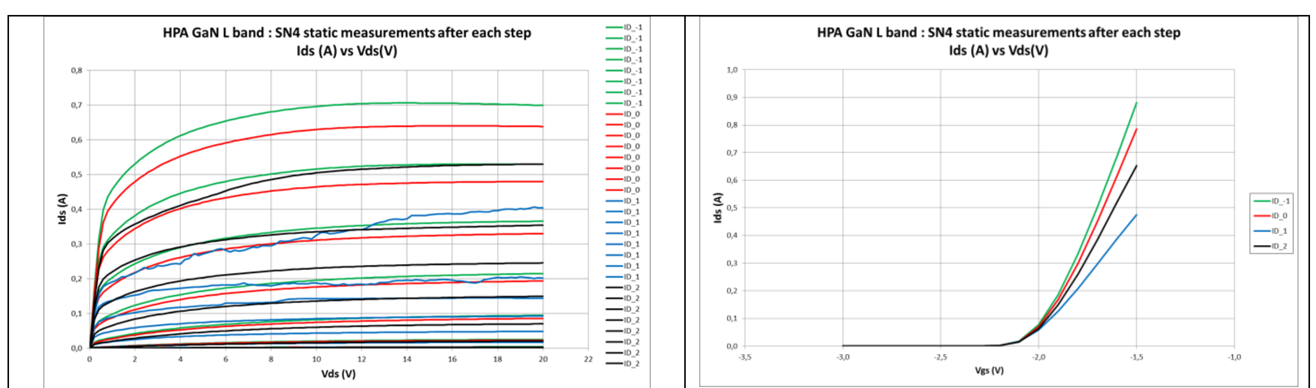

Figure 154 : HPA-1 Run-2 module #4. Static measurements after each compression step of the RF step stress measurements

Regarding the compression parameter of 3dBc obtained at NPR=15dB: the RF step stress measurements have been performed up to 5dBc gain compression for two HPA modules (One HPA module destroyed during RF step measurement due to parametric oscillations). No degradation has been observed on dynamic performances, showing that high level of compression could be used.

3. DEVELOPMENT OF KU-BAND MMIC GH25 HPA MODULES (HPA-2 MODULE)

3.1 Market trends survey

TAS-F has conducted a survey in order to give a more accurate picture (future) of the market trends for telecom application in Ku-band and to better justify the targeted SSPA equipment applications. A detailed justification in collaboration with the TAS SSPA product line, the TAS Telecom and Equipment Business Segment has been prepared. Two markets are identified: TX for TTC and SSPA for Telecom.

- Regarding TX for TTC applications in Ku-band, the main characteristics of the

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market which is targeted:
- Required quantity: 8x equipment to be delivered per year
- Pout>20W in CW mode

- Regarding GaN LC-SSPA for Telecom in Ku-band:
  - Objective would be to replace current LCTWTA solutions
  - Expected quantity: 200x SSPA to be delivered per year
- Regarding satellites constellation for Ku-band internet data application:
  - Pout>20W in CW mode
  - Pout=10W in multi-carrier mode at 15dB
  - Expected quantity: 900x satellites

Frequencies bandwidth for TX and Telecom SSPA are the same: 10.7 to 12.95GHz to be cover in two sub-bands. One Ku-band GaN HPA module would be used as output stage of the TX equipment . The same Ku-band GaN HPA module would be used as elementary building block of the output power section of the LC-SSPA. Based on this market trends activity, new electrical specifications are proposed for the Ku-band HPA module.

3.2 HPA specifications

This activity is dedicated to the definition of the HPA-2 baseline design and the transistor level requirements to achieve the following technical performances :
In First table are provided the initial specifications from the ESA SoW. In this document, the electrical analysis and thermal simulations are based on the preliminary HPA design based on these initial specifications
In second Table 2 are provided the new specifications from TAS requirements. Through a new CCN, TAS has proposed new specification for the Ku-band HPA. The market trends survey has been performed for Ku-band Telecom applications justifying the needs to adapt the specification of the HPA modules to the new requirements. Market trends survey results have presented in the previous chapter. In WP5300, the detailed design of the HPA module will be based on these specifications.

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Performance within Environmental Requirements	Ku-Band HPA-2 Value	Test Conditions	C/NC	Proposed Value	Comments
Nominal Output power with Multicarrier Signal	>6W	@ 15dB NPR Worst case over temperature	C		
Power Added Efficiency with Multicarrier Signal	>25%	@ 15dB NPR Worst case over temperature	C		
Centre Frequency	11,9 GHz	Ku-band	C		
Bandwidth	>1GHz	@ Nominal output power	C		
Gain Flatness	+/- 0.3 dB	Over the whole BW for fixed input power	C		
Gain with Multicarrier Signal	> 15 dB	@ Nominal output power	C		
Gain Compression Level with Multicarrier Signal	Max 2dB	@ 15dB NPR Worst case over temperature	-	Max 7dB	@ 15dB NPR Worst case over temperature
Maximum Phase shift	<15 deg	From 30 dB back-off to 4dB compression	-	<30deg	
Deviation from Linear Phase	6 deg pk-pk	versus frequency within BW	C		
Input Reflexion coefficient	<-10 dB	@ Nominal output power, over BW	C		
2nd harmonic rejection	>30 dBc		C		
Main DC voltage supply	>40V		-	22,5V	Value confirmed with UMS
Temperature	-10deg /+85deg		C		
Pressure	Ambient and 10e-6mbar		C		Multipactor free operation will be demonstrated by calculation with a sufficient margin

Table 25 : HPA-2 Specifications (initial version from ESA proposal)

Performance within Environmental Requirements	Unity	Specification Min		Max	Ku-Band HPA Test Conditions	Comments
Nominal Output power with CW signal	dBm	43	44		Max PAE	
Operating frequency	GHz	11,5		13	Ku-band	
Gain Flatness	dB			+/- 0.3	Over the whole BW for fixed input power	
Gain with CW Signal	dB	16			@ Nominal output power, over operating frequency bandwidth	
Gain Compression Level with CW Signal	dB			5	Max PAE	
Power Added Efficiency	%	42	45			**Ideal target 50% of PAE**
Maximum Phase shift	deg			15	From 30 dB back-off to 5dB compression	
Deviation from Linear Phase	deg pk-pk			6	versus frequency within operating frequency bandwidth	
Output Reflexion coeficient	dB			-10		
Input Reflexion coefficient	dB			-15		
2nd harmonic rejection	dBc	30			@ Nominal output power, over operating frequency bandwidth	
Main DC voltage supply				30V		Value confirmed with UMS
Temperature	deg	-10		85		
Pressure	mbar	Ambient and 10e-6mbar				Multipactor free operation will be demonstrated by calculation with a sufficient margin

Table 26 : New HPA-2 Specifications after CCN

3.3 Baseline Design

3.3.1 Loadpull simulations

The optimum operating class depends on the application area, this high power amplifier discussed in this work is designed for space application. The requirements are both output power and high power added efficiency at same time. So the class-AB is the best to fulfill this requirements. In our design, both of the transistors (stage 1&2)

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have been biased at 80mA/mm (deep AB class) to ensure PAE performances. This biasing point also guaranties an accurate non-linear simulation: the transistor model will be developed at this biasing condition (WP5200 performed by AMCAD).
Load-pull simulations have been undertaken to evaluate 8x100µm and 8x125µm GH25 transistor performances. To reach the maximum possible PAE performances, the following simulation procedure has been applied for each transistor at a given biasing point:

- Input impedance determination to maximize injected input power (close to perfect matching)
- Load pull at fundamental frequency to highlight maximum output power and PAE, harmonics 2 and 3 are set to 50 ohms
- Harmonic 2 load-pull optimization to maximize PAE performances, H1 set to optimal impedance previously fund and H3 set to 50ohms
- Re-optimization of H1, with H2 fixed to impedance exhibiting the maximum PAE performance, H3 on 50ohms.
- Harmonic 3 is not optimized, no significant influence on PAE due to its very high frequency

GH25 technology enables designs up to 30 (AMR) of drain voltage. In the following study, spatial de-rating ratio of 75% has been applied regarding AMR drain voltage, leading to a maximum biasing drain voltage VDS0 = 22.5V. This value has been consolidated by UMS.
Starting from the following biasing conditions:

- IDS0 = 50mA/mm
- VDS0 = 22.5V (Maximum drain voltage derated at 75%). During the study and based on updated information from UMS, Vds0 will be increased to 30V. Thus, detailed design, manufacturing and test will be based on 30V.

Load-pull analysis have been undertaken at 12.5GHz (higher frequency) following the specific methodology previously detailed and have highlighted the following performances. According to the GH25_10 v1.2 DK, load-pull simulations have been done at transistor level. The results of the 8x125µm load-pull analysis with harmonic 1 and harmonic 2 optimization is given below :

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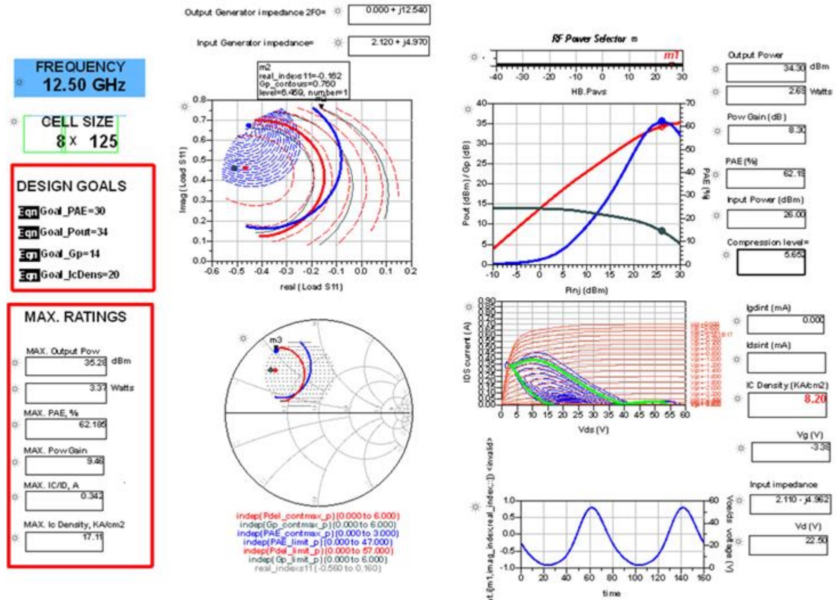

Figure 155 : Loadpull simulation of GH25 8x125µm transistors

For 8x125µm transistor, PAE peak of 62% was simulated with optimum output load at fundamental and second harmonic frequencies (H3 set to 50ohms).

3.3.2 MMIC architecture

PAE performances were considered of primary importance in the frame of this demonstrator. As a consequence this high power amplifier (HPA-2) has been designed to maximize the power added efficiency (PAE) performances. Single-ended configuration was chosen since the required narrow bandwidth (nearly 10%around the center frequency) allows to meet the requirements avoiding balanced solutions (which would require larger chip size). Transistor size of 8x125µm exhibits the best PAE / output power trade-off with a maximum peak PAE of 62% associated to an output power of 34,3dBm. The active device periphery best configuration has been found out to be:

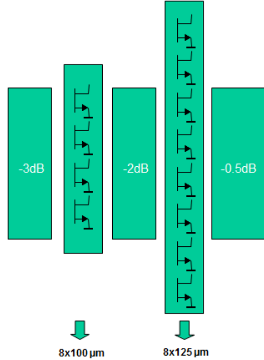

Figure 156 : Preliminary topology of the GH25 HPA-2

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The HPA topology is based on two stages of amplification with an arborescent structure. Two stages were required to reach the power gain of 15dB at nominal operating point with multi-carrier signal.
The active device periphery best configuration (for both designs) has been found out to be:

- Stage 1 : 4 x 8x100µm
- Stage 2 : 8 x 8x125µm

3.3.3 RF performance simulation

Non-linear simulations have been performed using Volti software with the following setup :

- Use of AMAM / AMPM / AMPdc curves from loadpull simulations of 8x100µm and 8x125µm transistors
- Input power : -10 to 34dBm
- Center Frequency : 12.5GHz

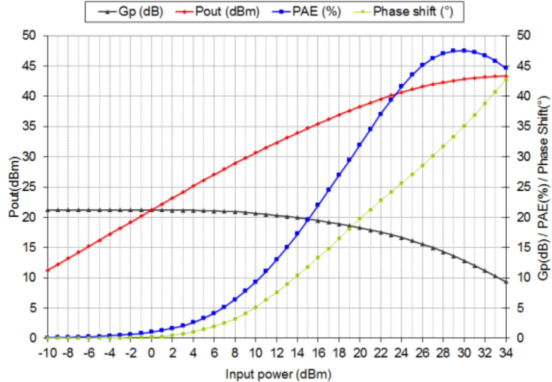

Figure 157 : Performance versus Pin in CW mode of the GH25 HPA-2. Vds=22,5V, RFfreq=12.5GHz

With multi-carrier signal, contribution of each parts of the GH25 HPA-2 module is presented in the next table. Simulation results are presented at NPR=15,2dB.

RF SECTION		Gain	Cumul Gain	Signal Level	Signal level	Linearity	Pdc	Pdiss	PAE	Gain Comp
N°	Elements	dB	dB	dBm	W	dB	W	W	%	dB
	INPUT			22,00	1,58E-01					
1	INPUT	-3,00	-3,00	19,00	0,0794	285,19	0,00	0,08	0,00	0,00
2	4x8x100	11,74	8,74	30,74	1,1847	22,12	4,34	3,23	25,48	1,57
3	INTERSTAGE	-2,00	6,74	28,74	0,7475	22,12	0,00	0,44	0,00	0,00
4	8x8x125	10,53	17,27	39,27	8,4454	15,25	17,28	9,58	44,55	2,87
5	OUTPUT	-0,50	16,77	38,77	7,5270	15,25	0,00	0,92	0,00	0,00
Total RF Section			16,77	38,77	7,53	15,25	21,61	14,25	34,09	4,45

Table 27 : Performance in multi-carrier mode of the GH25 HPA-2. Vds=22,5V, RFfreq=12,5GHz

With a multi-carrier signal, at NPR=15,2dB, the PAE performance match the required performance with a PAE of 34%. At NPR=15,2dB, output power is 48,77dBm (7,53W).

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3.3.4 Packaging solution

An existing Ku-band dissipative hermetic package based on CuW material will be used for the assembly of the HPA-2 module. Layout of the package including preliminary HPA-2 is given hereafter. This package is space compliant and have been developed by TAS. Baseplate material is CuW. This Ku-band package have also been designed taking into account both electrical and mechanical design constraints, multipactor and DC current constraints on RF feedthrough. CuW baseplate and relevant interface optimization have demonstrates up to 200 W/mK thermal resistance. In future, TAS expects to develop a new Ku-band high dissipative package based on CuD material

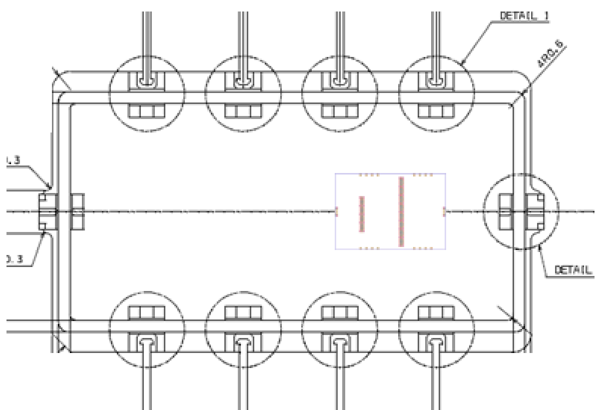

Figure 158 : Layout of the Ku-band hermetic package including preliminary MMIC HPA-2

3.3.5 Thermal simulations

Thermal analysis on the GH25 HPA-2 module including the transistor physical description and packaging environment will be launched in order to evaluate junction temperature. The thermal behavior of the 0.25µm device represented by a multi-port inputs and outputs SPICE thermal circuit will be generated and used for non-linear modeling activities. Several cases will be studied to provide to the designer an overview in terms of thermal performances.
Two different baseplate materials will be considered for thermal simulation.

- CuW with K=210W/m/°C
- CuD with K=400W/m/°C

Description of the thermal stack used in thermal simulation is provided below

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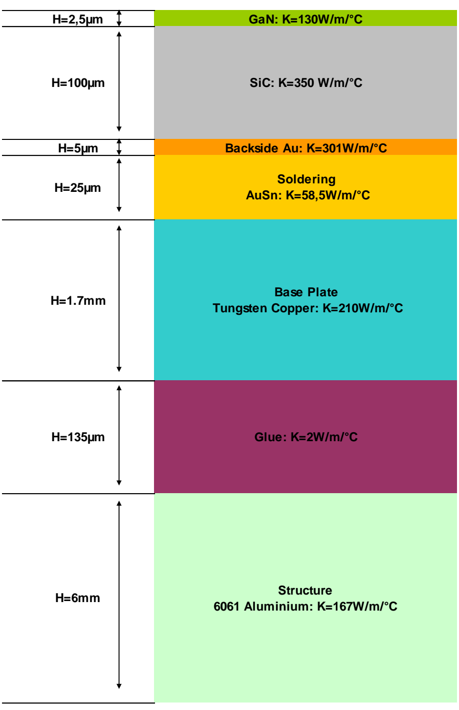

Figure 159 : Description of the thermal stack used for thermal simulation: baseplate material of the package: CuW

In this paragraph, thermal simulations results are provided for second transistor stage.

3.3.5.1 Thermal study of GH25 8x125µm transistor

The mesh of the device is presented in Figure 160 after simplification for symmetry consideration. Simulation has been performed for several baseplate temperatures (25°C, 50°C, 75°C, 100°C). The dissipated power in the ¼ of the device is 0.25W. Materials are supposed to be linear excepted GaN material which is nonlinear.
Figure 160 show the temperature map for different baseplate temperatures. Figure 160 presents also the temperature along a line in the channel layer. The following table reports the values for temperature and thermal resistances in the devices. The thermal resistance is around 11.8°C/W with a small variation of 5% due to materiel non-linearity.

Baseplate temperature (°C)	25	50	75	100
Dissipated power(W)	1	1	1	1
Thermal resistance (°C/W)	11.6	11.81	12.02	12.21
Temperature (°C)	36.6	61.81	87.02	112.21

Table 28 : GH25 8x125µm transistor. Thermal resistance(°C/W) for various base plate temperatures and dissipated power.

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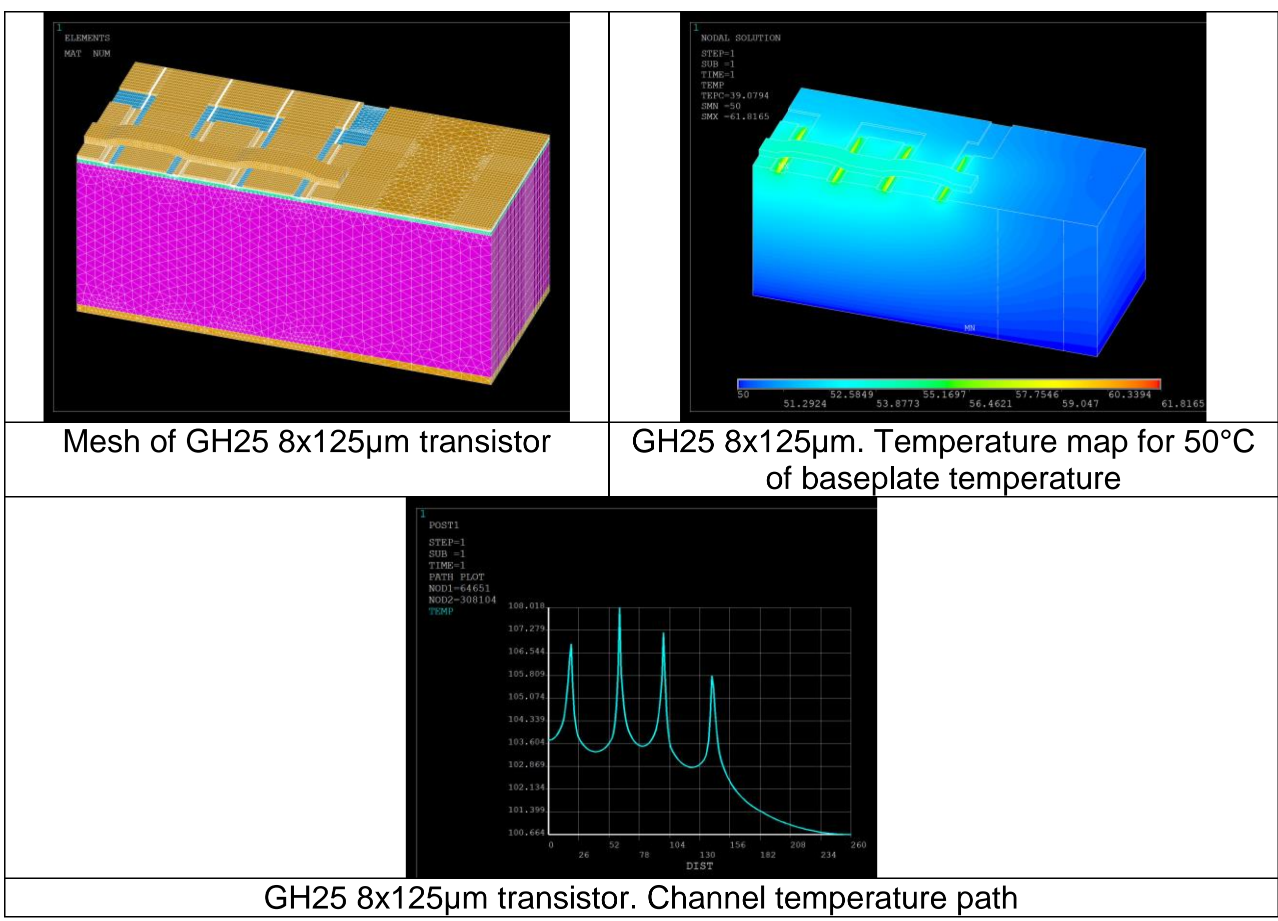

Mesh of GH25 8x125µm transistor

GH25 8x125µm. Temperature map for 50°C of baseplate temperature

GH25 8x125µm transistor. Channel temperature path

Figure 160 : 8x125µm transistor thermal simulations

3.3.5.2 Thermal study of the GH25 8x8x125µm power-bar

The mesh of the device is presented in figure below after simplification for symmetry consideration. Simulation has been performed for several baseplate temperatures (25°C, 50°C, 75°C, 100°C). The dissipated power in the ¼ of the device is 2.5W corresponding to 10W in the whole device. Figure below shows also the temperature map for different baseplate temperatures. The following table reports the values for temperature and thermal resistances in the devices.
The thermal resistance is around 1.48°C/W with a small variation of 5% due to materiel non-linearity.

Baseplate temperature (°C)	25	50	75	100
Dissipated power(W)	10	10	10	10
Thermal resistance (°C/W)	1.46	1.48	1.50	1.53
Temperature (°C)	39.59	64.84	90.10	115.34

Table 29 : GH25 8x8x125µm power-bar. Thermal resistance(°C/W) for various base plate temperatures and dissipated power.

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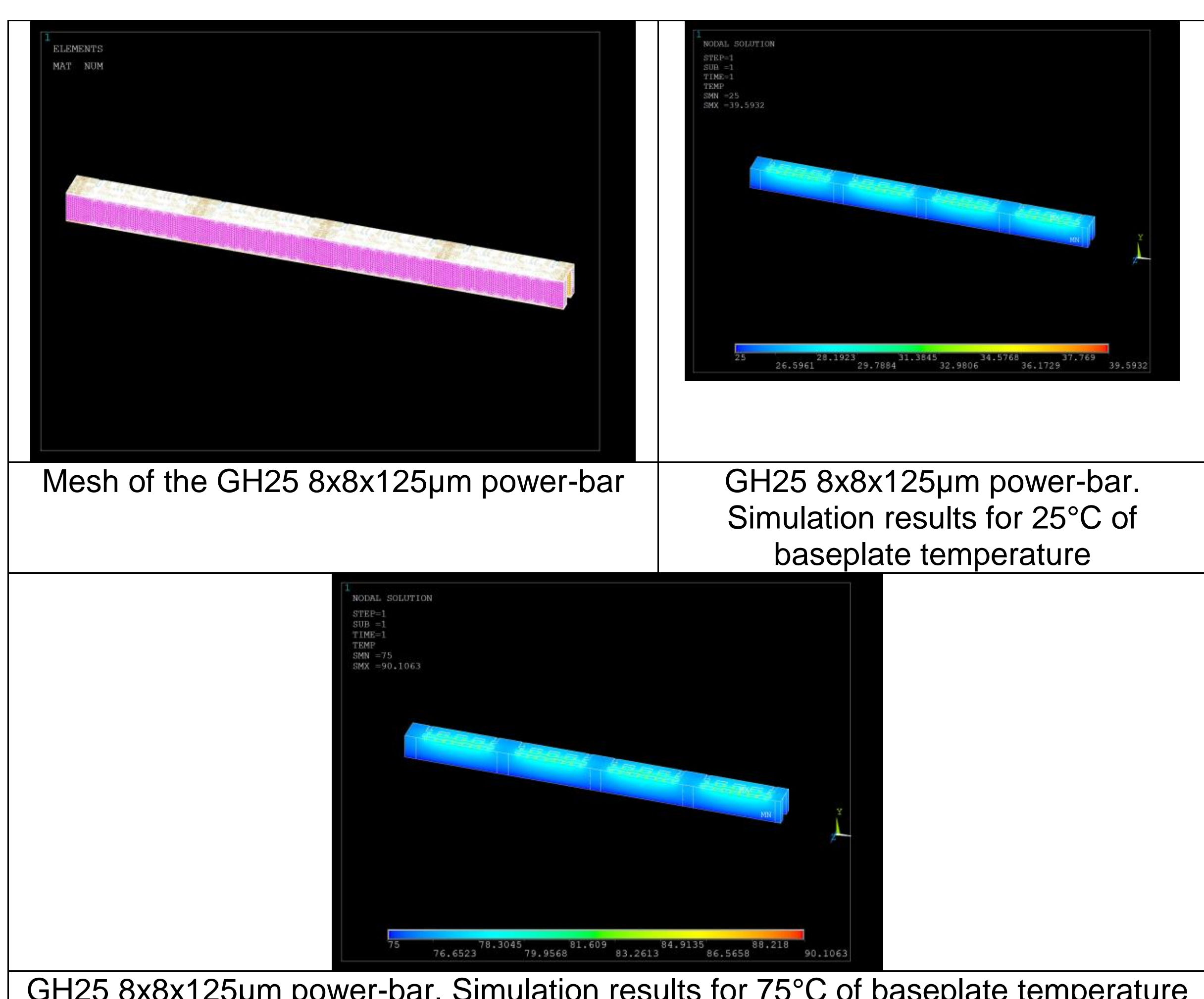

Mesh of the GH25 8x8x125µm power-bar	GH25 8x8x125µm power-bar. Simulation results for 25°C of baseplate temperature
GH25 8x8x125µm power-bar. Simulation results for 75°C of baseplate temperature	

Figure 161 : 8x8x125µm transistor thermal simulations

3.3.5.3 Thermal study of the packaging of the power amplifier

In this part, we consider the part of the thermal stack presented in Figure 159 corresponding to the packaging. Each power-bar is replaced by a rectangle. The dimensions of the rectangle correspond to the footprint of the power-bar. The mesh of the structure is presented in figure below. The thermal network is extracted by injecting power in first and second stage alternatively. Results are presented in figures below. Validation is proposed by injecting power simultaneously in both stages as shown in Figure 162

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Mesh of the packaging	Injection in stage 1 (1.65W in ½ stage)
Injection in stage 2 (4.61W in ½ stage)	Validation of thermal matrix

Figure 162 : Thermal study of the packaging

3.3.5.4 Temperature evaluation

Hypothesis for thermal calculation is presented below :
Tr = transistor of stage 1 or 2
Rth packaging = matrix of thermal resistances

Tj1, Tj2 = temperature of transistor in stage 1, stage 2
Tbase = T baseplate
Tp1, Tp2 = Tpackaging under powerbar1 or 2
Rj1=14.5 (thermal resistance transistor of stage 1)
Rj2=11.8 (thermal resistance transistor of stage 2)
P1, P2= power in stage 1 or 2
Pj1, Pj2 = P1/4, P2/8

For CuW baseplate material:	For CuD baseplate material:

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• Z11=4.42°C/W • Z12=0.89°C/W • Z21=Z12 • Z22=2.93°C/W	• Z11=2.92°C/W • Z12=0.694°C/W • Z21=Z12 • Z22=1.97°C/W

For example, if you want to compute Tj1 or Tj2 (junction temperature of transistor in stage 1 or transistor in stage 2), calculation is:

Case 1 : Pout_RF=7,53W NPR=15,25dB, Tbase=50°C, CuW material:

- Dissipated power in stage 1 : **3.2**W
- Dissipated power in stage 2 : **9.6**W

Tj1 = 14.5*Pj1+Tp1 = 14.5*0.8 + 4.42***3.2**+0.89***9.6**+**50**=84.3°C
Tj2 = 11.8*Pj2+Tp2 = 11.8*1.2 + 0.89***3.2**+2.93***9.6**+**50**=95.14°C

Case 2 : Pout_RF=7,53W NPR=15,25dB, Tbase=85°C, CuW material:

- Dissipated power in stage 1 : **3.2**W
- Dissipated power in stage 2 : **9.6**W

Tj1 = 14.5*Pj1+Tp1 = 14.5*0.8 + 4.42***3.2**+0.89***9.6**+**85**=119,3°C
Tj2 = 11.8*Pj2+Tp2 = 11.8*1.2 + 0.89***3.2**+2.93***9.6**+**85**=130,1°C

Case 3 : Pout_RF=7,53W NPR=15,25dB, Tbase=85°C, CuD material:

- Dissipated power in stage 1 : **3.2**W
- Dissipated power in stage 2 : **9.6**W

Tj1 = 14.5*Pj1+Tp1 = 14.5*0.8 + 2,92***3.2**+0.694***9.6**+**85**=112,6°C
Tj2 = 11.8*Pj2+Tp2 = 11.8*1.2 + 0.694***3.2**+1,97***9.6**+**85**=120,3°C

3.4 0.25µm Technology Modelling and Performance

In this chapter, first part synthesizes AMCAD Engineering I(V) / S-Parameters and Load Pull measurements achieved on the GH25 transistors 8x125µm. For this study, UMS provided four samples of GH25 transistors. Second part synthesizes AMCAD Engineering modelling activity achieved on the GH25 transistors 8x125µm

3.4.1 Unitary cell measurements

The system set up for the transistor (8x100µm, 8x125µm GH25 UMS) characterization is described below. The bias voltages and S-parameters are performed in CW mode.

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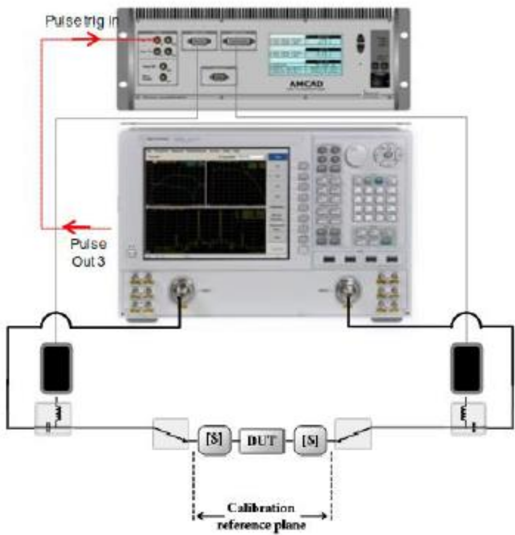

Figure 163 : AMCAD I(V) and [S] test bench for transistors characterizations

The principle of measurement pulse is to describe the I(V) network by quasi-isothermal measurements using short pulses around a quiescent bias point selected. The quiescent bias point of rest is provided by the voltage levels and Vgs0 vds0. This results in a current Ids0 polarization. Pulses, whose levels are represented by VGSI, IGSI, VDSI IDSI and describe all the characteristics of input and output of the transistors.

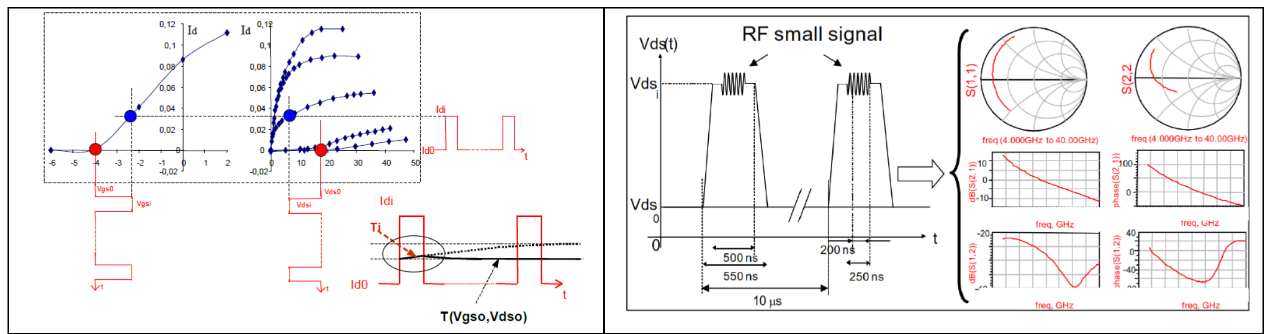

Figure 164 : Typical timings (DC bias / RF) used for pulsed measurements

4 samples for each development are supplied by UMS:
- 8x100 -> Ref: N17, T12, T7, N12
- 8x125 -> Ref: N17, T12, T7, N12

Preliminary continuous I(V)/RF measurements have been performed on each development in order to estimate the process dispersion and to select the most representative samples for the complete characterizations. These dispersive measurements have been performed at ambient temperature (25°C). The results for the different transistor have shown that the representative sample is referred T7.
In this final report, results are presented only for 8x125µm transistor size.

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In figure below are presented the results for Quiescent bias : Vds0=0V, Vgs0=0V. Idss is reduced by 8% to a rise of 75 °C the chuck temperature

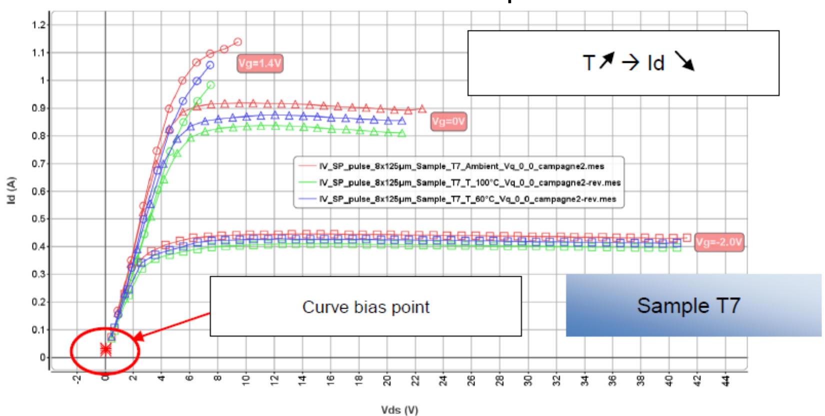

Figure 165 : Output current with different chuck temperature (25°C, 60°C, 100°C), transistor 8x125 GH25 measurements (bias points Vds0=0V, Vgs0=0V)

In figure below are presented the results for Quiescent bias : Vds0=27V, Ids0 = 50mA/mm. Idss is reduced by 8% to a rise of 75 ° C the chuck temperature.

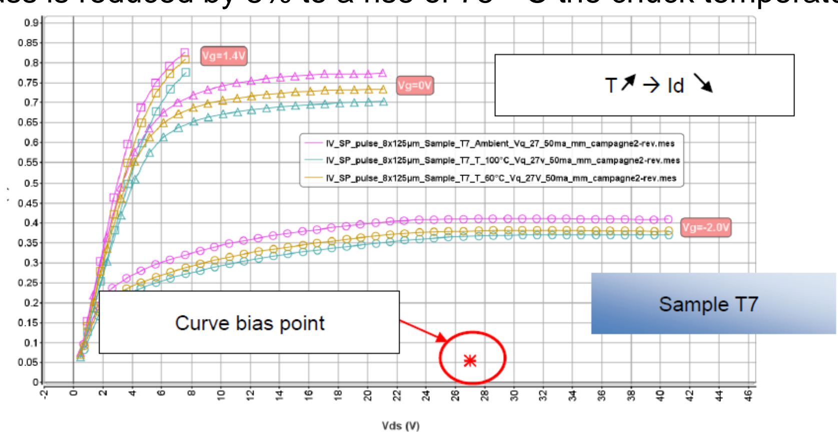

Figure 166 : Output current with different chuck temperature (25°C, 60°C,100°C), transistor 8x125 GH25 measurements (bias points Vds0=27V, Ids0=50mA)

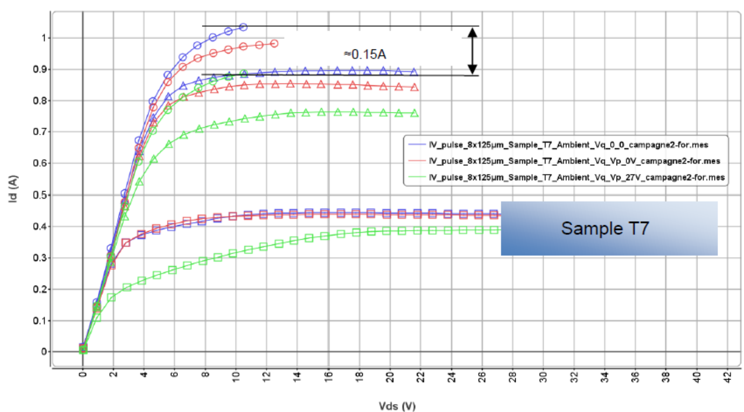

Figure 167 : Highlighted phenomena traps

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Regarding the phenomena traps, the effect on the output characteristic is a reduction of the drain current of 14%

Measurement for classical AB class (Vds0=27V, Ids=50mA/mm) is presented below.

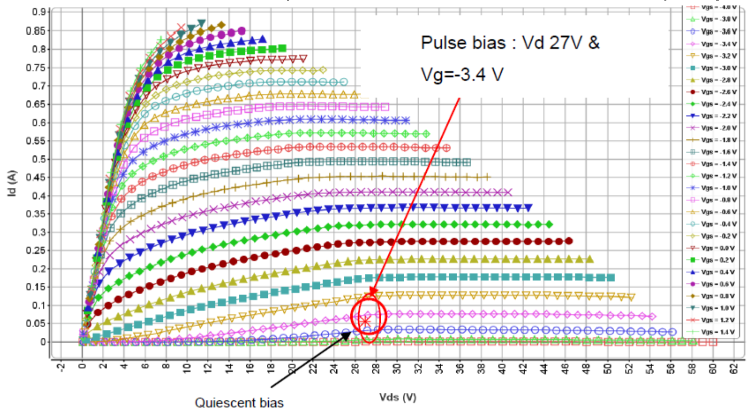

Figure 168 : Output current, quiescent bias: (27V, 50mA), (chuck temperature = 25°C), transistor 8x125 GH25

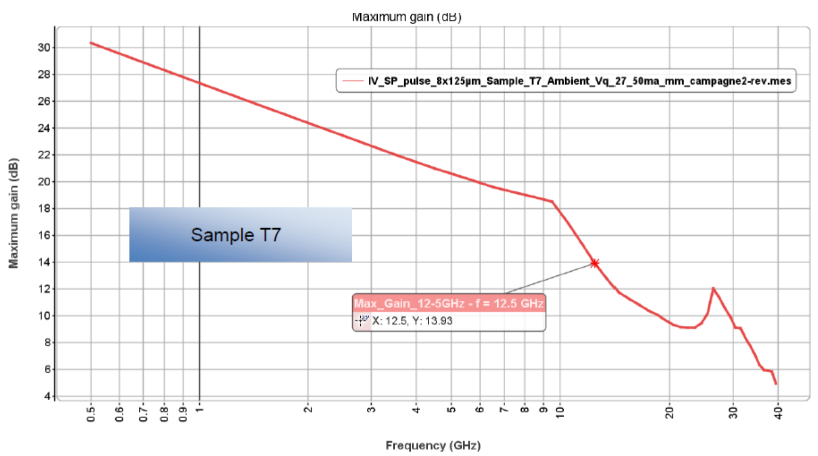

Figure 169 : Maximum Gain @ Vds0=27V, Ids0=50mA

The loadpull system set up for the devices characterization is described below

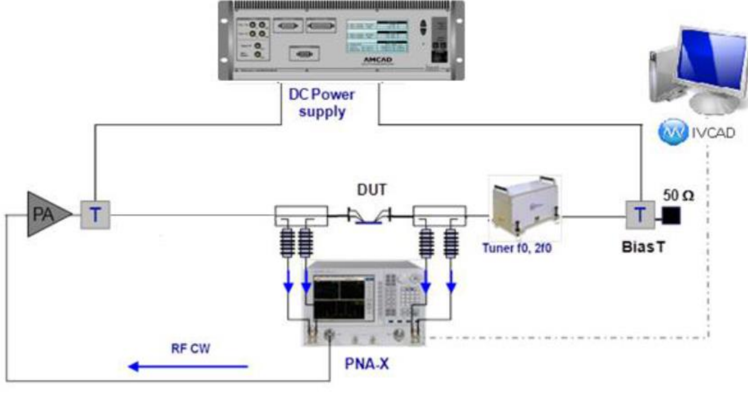

Figure 170 : AMCAD VNA-based load-pull system

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The objective is to find the optimal load impedance power added efficiency (PAE) for f0 = 12.5GHz CW mode for Pout > 3W/mm.
The loadpull methodology used for performance optimization is :

- Measurement and optimization of f0 load impedance
- Measurement and optimization of 2f0
- Re-optimization of f0 load impedance

Final performance obtained after loadpull optimization are presented below:

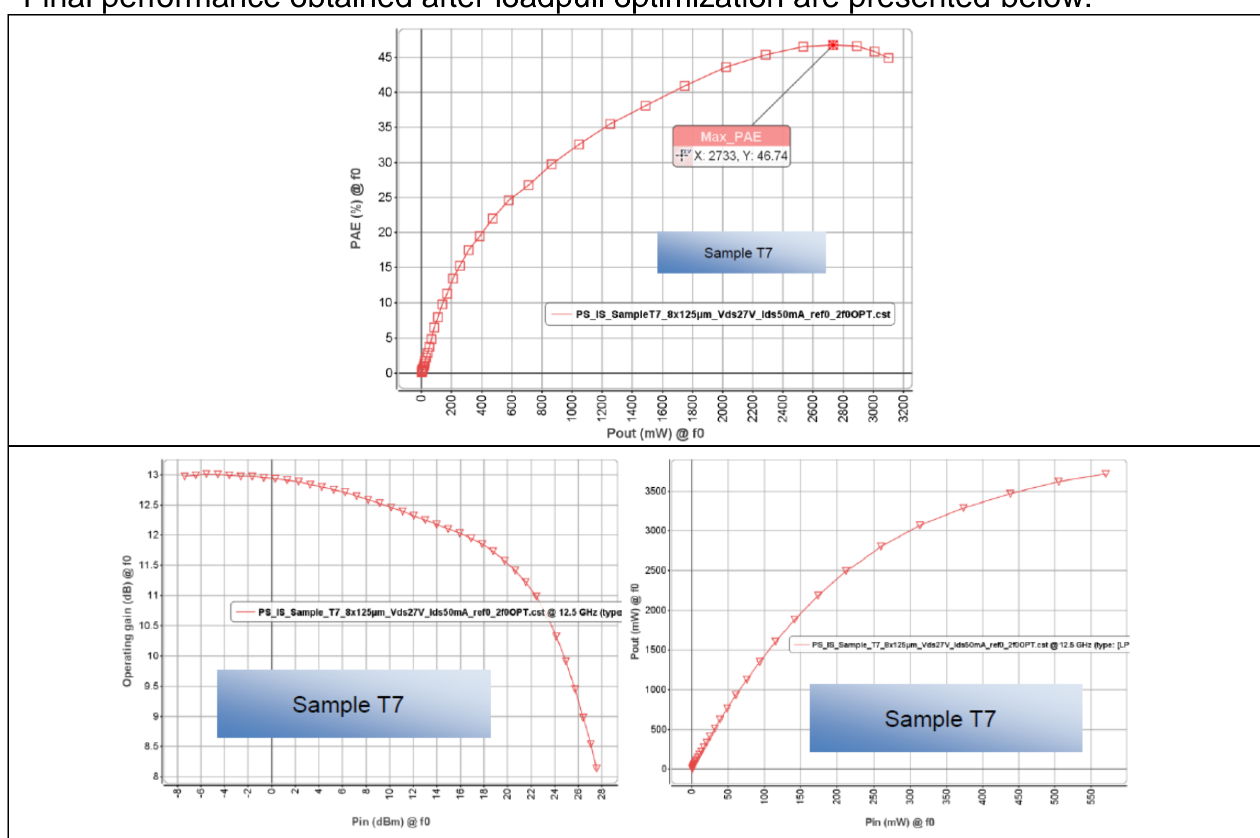

Figure 171 : 8x125µm performance at 12.5GHz after loadpull optimization

Development	Linear Gain (dB)	Output Power (W)	PAE foOPT (%)	PAE AllOPT (%)	Zload f0 opt PAE (Ω)	Zload 2f0 opt PAE (Ω)	Zsource (Ω)
8x125µm	12.97	3.180	46.45	47.31	10.19+j23.39	4.85+j25.69	50

Table 30 : 8x125µm performance at 12.5GHz after loadpull optimization

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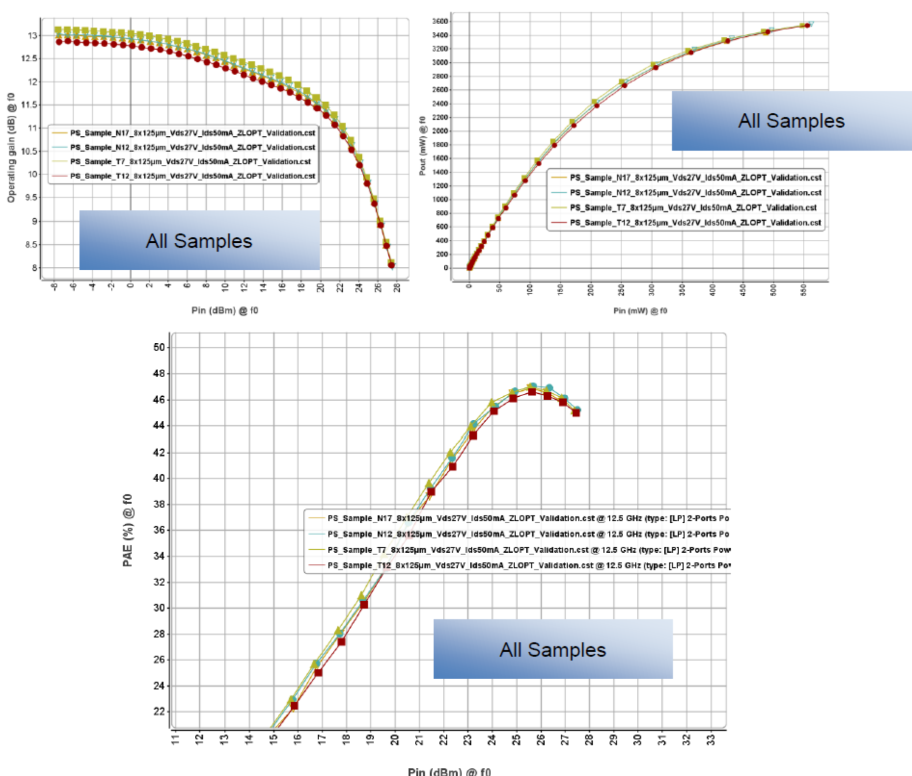

Figure 172 : Sample dispersion for optimal PAE load impedances @ 12.5GHz (Vds=27V, 50mA)

Sample	Linear Gain (dB)	Output Power (W)	PAE max (%)	Zload f0 opt PAE (Ω)	Zload 2f0 opt PAE (Ω)	Zsource (Ω)
T7	13.13	3.46	47	9.26+J23.33	8.87+j26.11	50
N12	13.04	3.47	47.1	9.26+J23.33	8.87+j26.11	50
N17	13.01	3.44	46.9	9.26+J23.33	8.87+j26.11	50
T12	12.87	3.45	46.6	9.26+J23.33	8.87+j26.11	50

Figure 173 : Synthesis of sample dispersion for optimal PAE load impedances @ 12.5GHz (Vds=27V, 40mA)

3.4.2 Unitary cell modeling activity.

The provided model is a 3 ports transistor. All the parameters are available as well as the chuck temperature and selfheating effects

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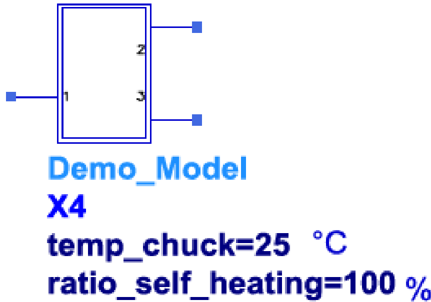

Figure 174 : 3 ports transistor model

The model is adjusted through several measurements (I(V), [S], load-pull...) in different operating conditions (bias, temperature, frequency...) in order to have a coherent model. Comparisons between the pulsed I(V) measurements and the model @ T_chuck=25°C are illustrated below, for the quiescent bias conditions : Vds0=27V, Ids0=50mA.

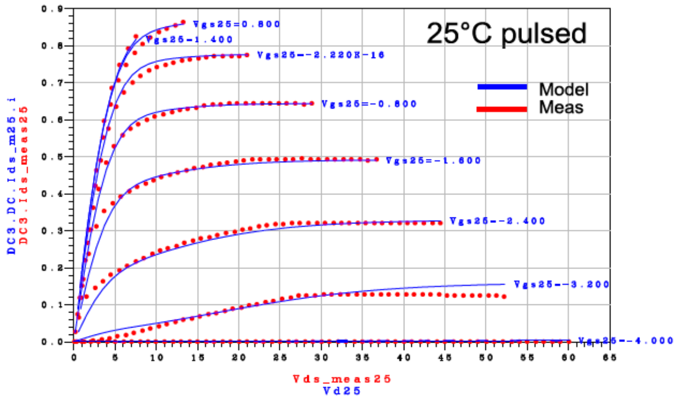

Figure 175 : Meas. vs Model 8x125µm @ 25°C

Thermal resistance Rth is extracted from DC and pulsed measurements at ambient temperature and 100°C respectively. For the same Vgs, the intercept of the two curves describe the same thermal state.

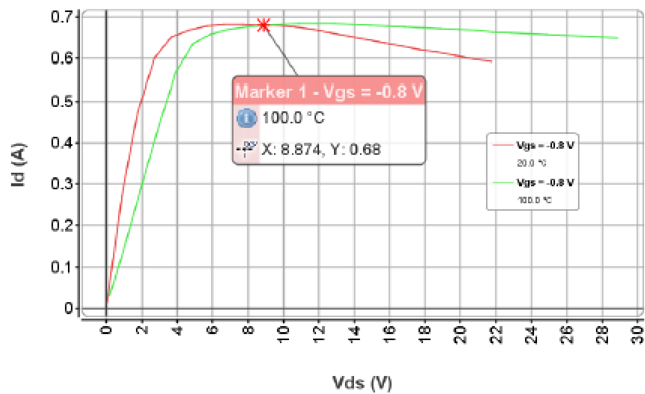

Figure 176 : Thermal resistance extraction for 8X125µm

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Finally, thermal parameters of the model are extracted from measurements at ambient and 100°C in pulsed mode. Thermal dependence is then implemented to the relevant elements such as the drain current which is directly impacted.
Comparisons between the pulsed I(V) measurements and the model @ Tchuck = 60°C &100°C are illustrated below, for the quiescent bias conditions : Vds0=27V, Ids0=50mA.

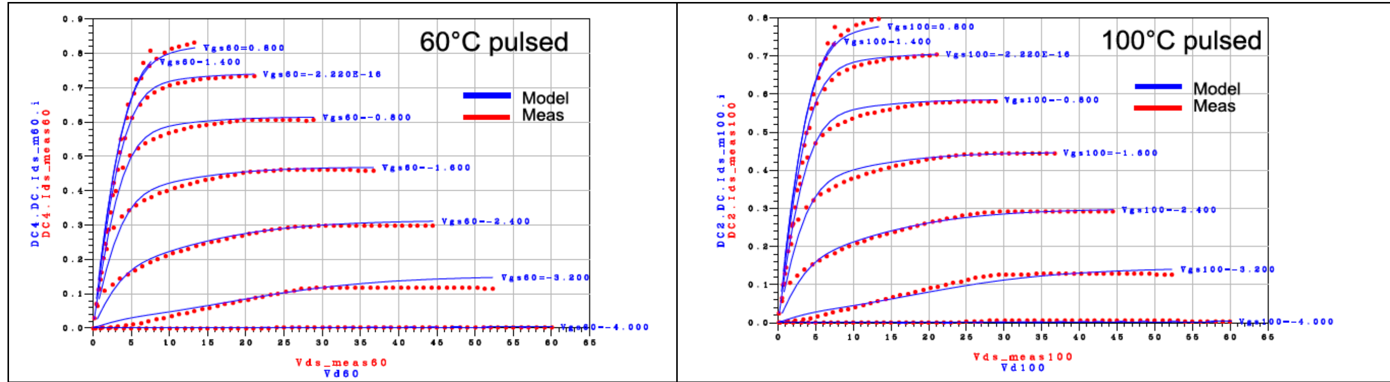

Figure 177 : Meas. vs Model 8x125µm @ 60°C

For S parameters [0.5 to 39.5 GHz] validation, the model is compared to the measurement on several bias points.

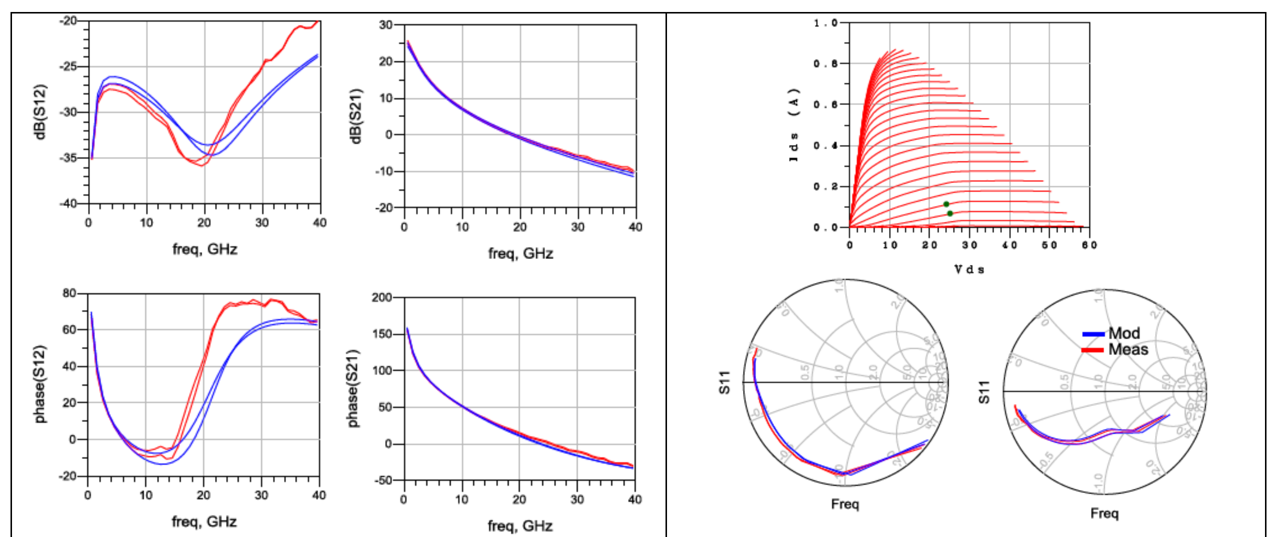

Figure 178 : [S] parameter Meas. vs Model 8x125µm @ 25°C

In Load-pull configuration, the comparison is performed at one frequency (12.5GHz) and for several load impedances including the optimum ones. Next figure illustrates contour of max PAE @ 3dB respectively.

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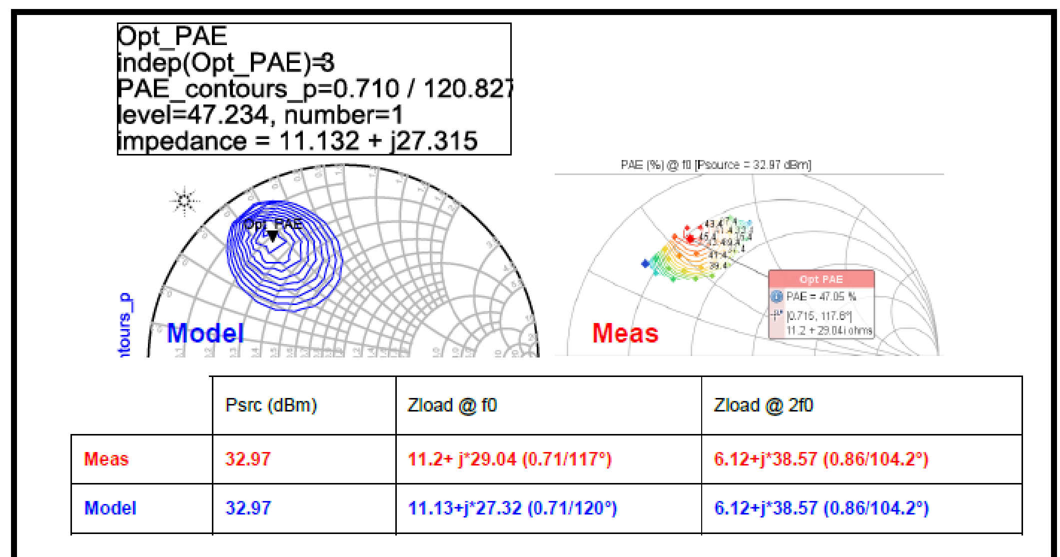

	Psrc (dBm)	Zload @ f0	Zload @ 2f0
Meas	32.97	11.2+ j*29.04 (0.71/117°)	6.12+j*38.57 (0.86/104.2°)
Model	32.97	11.13+j*27.32 (0.71/120°)	6.12+j*38.57 (0.86/104.2°)

Figure 179 : Contour of Max PAE - Meas. vs Model 8x125µm

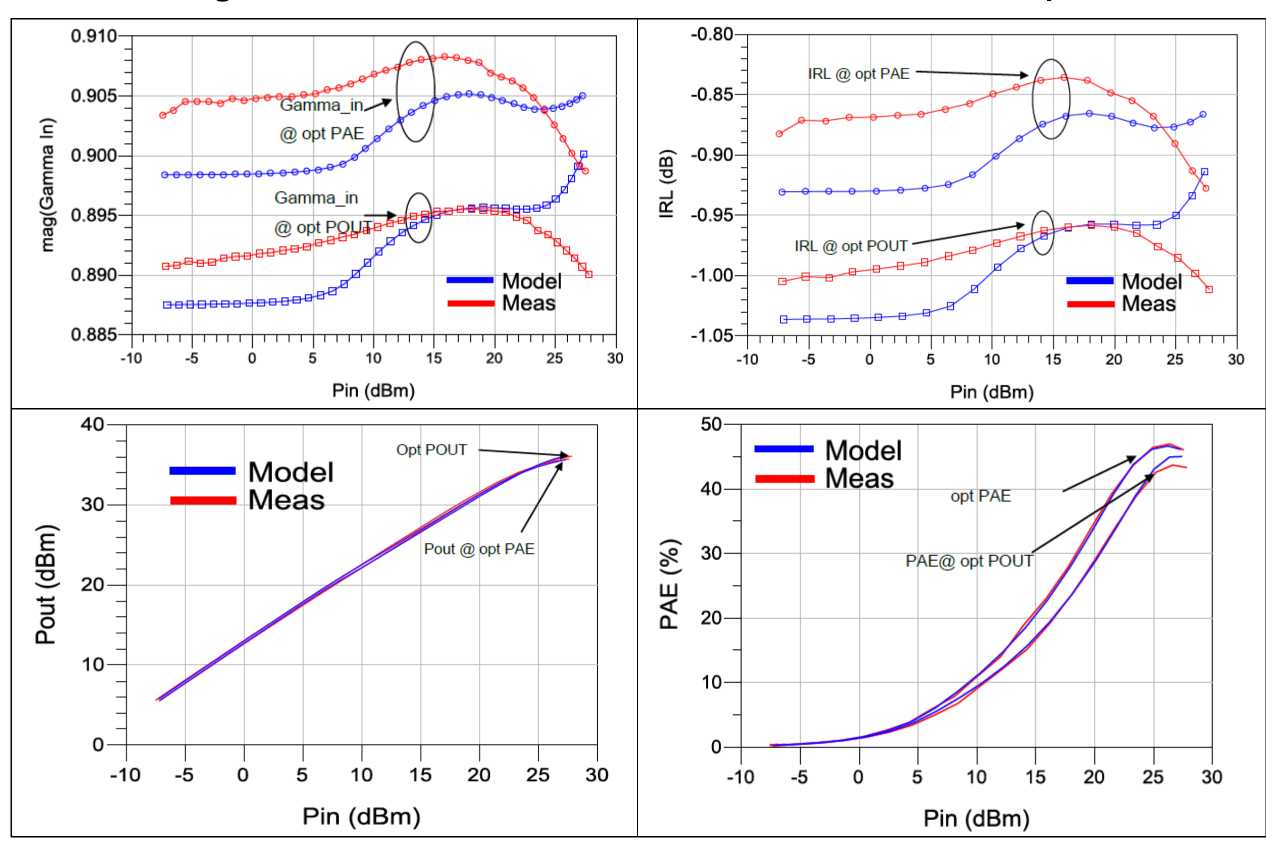

Figure 180 : Gamma_in / IRL / Pout / PAE - Meas. vs Model 8x125µm

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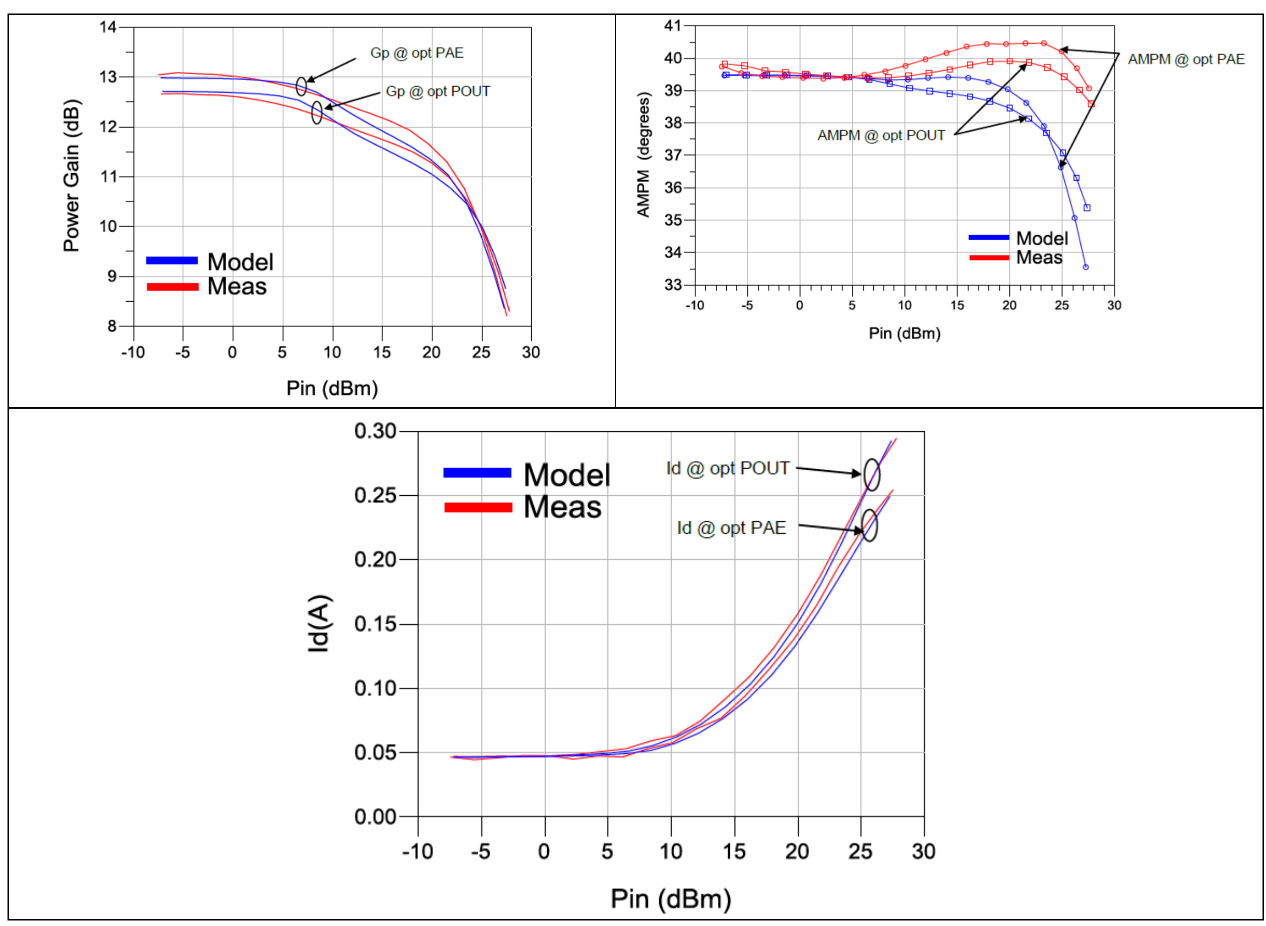

Figure 181 : Power Gain / AM-PM / Id - Meas. vs Model 8x125µm

3.5 Detailed Design

Three versions have been designed and are presented in this chapter

- Version 1: HPA-2 module which is a Class AB Ku-band GH25 MMIC HPA module has been finalized with NL electrothermal model of the transistor cell provided by AMCAD.
- Version 2: Doherty Ku-band GH25 MMIC HPA module has been designed using NL electro-thermal model of the transistor cell from the UMS DK
- Version 3: Doherty Ku-band GH25 MMIC-Hybrid HPA module has been designed using NL electro-thermal model of the transistor cell from the UMS DK

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Regarding these three HPA versions, a common electrical specifications matrix has been used and is recalled below:

		Specification			Ku-Band HPA	
Performance within Environmental Requirements	**Unity**	**Min**		**Max**	**Test Conditions**	**Comments**
Nominal Output power with CW signal	dBm	43	44		Max PAE	
Operating frequency	GHz	11.5		13	Ku-band	
Gain Flatness	dB			+/- 0.3	Over the whole BW for fixed input power	
Gain with CW Signal	dB	16			@ Nominal output power, over operating frequency bandwidth	
Gain Compression Level with CW Signal	dB			5	Max PAE	
Power Added Efficiency	%	42	45			
Maximum Phase shift	deg			15	From 30 dB back-off to 5dB compression	
Deviation from Linear Phase	deg pk-pk			6	versus frequency within operating frequency bandwidth	
Output Reflexion coeficient	dB			-10		
Input Reflexion coefficient	dB			-15		
2nd harmonic rejection	dBc	30			@ Nominal output power, over operating frequency bandwidth	
Main DC voltage supply				30V		Value confirmed with UMS
Temperature	deg	-10		85		
Pressure	mbar	Ambient and 10e-6mbar				Multipactor free operation will be demonstrated by calculation with a sufficient margin

Table 31 : Specifications of the HPA-2 Module and Doherty HPA modules

3.5.1 Detailed Design of version 1 : HPA-2 module

PAE performances were considered of primary importance in the frame of this demonstrator. As a consequence this high power amplifier (HPA) has been designed to maximize the power added efficiency (PAE) performances. Single-ended configuration was chosen since the required narrow bandwidth (nearly 10%around the

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center frequency) allows to meet the requirements avoiding balanced solutions (which would require larger chip size).
According to the transistor mode provided by AMCD, load-pull simulations have been done at transistor level. Transistor size of 8x125µm exhibits the best PAE / output power trade-off with a maximum peak PAE of 48% associated to an output power of 36.3dBm. The active device periphery best configuration has been found out to be:

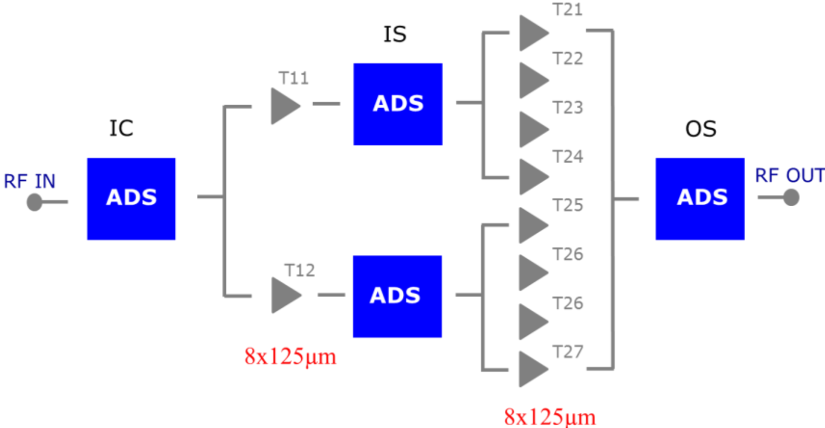

Figure 182 : HPA-2 module. Amplifier topology

The HPA topology is based on two stages of amplification with an arborescent structure. Two stages were required to reach the power gain of 17dB at compression level for 7dB of gain compression.

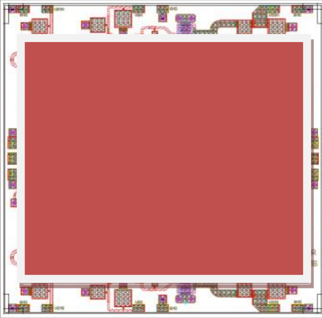

Figure 183 : HPA-2 module. MMIC circuit layout

Spiral inductors are used in matching-networks and for DC bias de-coupling. It is advised for high power amplifier to avoid inductors on output matching combiner and Drain bias voltage due to high current that will flow under small microstrip line width.

- The capacitors are crucial for the realisation of the matching networks and DC-decoupling networks. The capacitors used for this discussed high power amplifier is the MIM capacitor.This capacitor is formed by two metal plates on top of each other with a dielectric in between. The main features regarding passive elements of the GH25-10 technology are as follows:
- 30 W/ TaN thin film resistors
- 1000 W/ TiWSi thin film resistors

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- 250 pF/mm² MIM capacitors
- 1.8 µm evaporated and 7 µm electroplated gold layers for interconnects and lines
- Air bridges to overcome device topography and realization of integrated inductors
- SiN-protection of the wafer front side
- 100 µm substrate thickness and via interconnects for source contacting / connection tog round
- Pads

CW Harmonic Balance simulation have been performed with the non-linear transistor model realized by AMCAD for this specific 8x125 µm GH25 HEMT

At both input and output RF ports of the MMIC, two half-wires bonding have been considered to take into account a gap length of 650 µm from the MMIC RF PAD to the external 50 Ω line. A variation of ±33% of this equivalent inductance has been included in the statistical analysis. Simulation of the performances of the HPA have been also verified with a dedicated ADS DELF model representative of the RF connexion of the MMIC (input and output) to the hermetic package. At each DC PAD the simplified circuit shown below has been considered to model the connection of the MMIC with the extern circuit.

The optimum operating class depends on the application area, this high power amplifier discussed in this work is designed for space application. The requirements are both output power and high power added efficiency at same time. So the class-AB is the best to fulfil this requirements. In our design, both of the transistors (stage 1&2) have been biased at 50mA/mm (deep AB class) to ensure PAE performances. This biasing point also guaranties an accurate non-linear simulation: the transistor model has been developed at this biasing condition.

Regarding loadpull simulations, the following approach has been used:

- Load-pull simulations have been undertaken to evaluate 8x125µm GH25 transistor performances. To reach the maximum possible PAE performances, the following simulation procedure has been applied for each transistor at a given biasing point:Input impedance determination to maximize injected input power (close to perfect matching)
- load pull at fundamental frequency to highlight maximum output power and PAE, harmonics 2 and 3 are set to 50 ohms
- Harmonic 2 load-pull optimization to maximize PAE performances, H1 set to optimal impedance previously fund and H3 set to 50ohms
- Re-optimization of H1, with H2 fixed to impedance exhibiting the maximum PAE performance, H3 on 50ohms.
- Harmonic 3 is not optimized, no significant influence on PAE due to its very high frequency

Starting from the following biasing conditions:

- IDS0 = 50mA/mm
- VDS0 = 28V (leading to 30V (ROR) of drain voltage)

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Load-pull analysis have been undertaken at 12.25GHz (centre frequency) following the specific methodology previously detailed and have highlighted the following performances. The results of the load-pull analysis after optimization is given below :

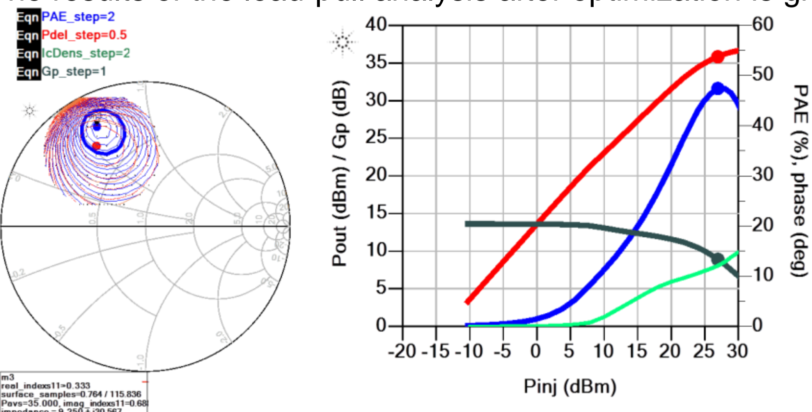

Figure 184 : Final load-pull optimization results

The S-parameter HPA simulation results, at biasing point condition equal to IDS0=50mA/mm and VDS=28V, are shown below:

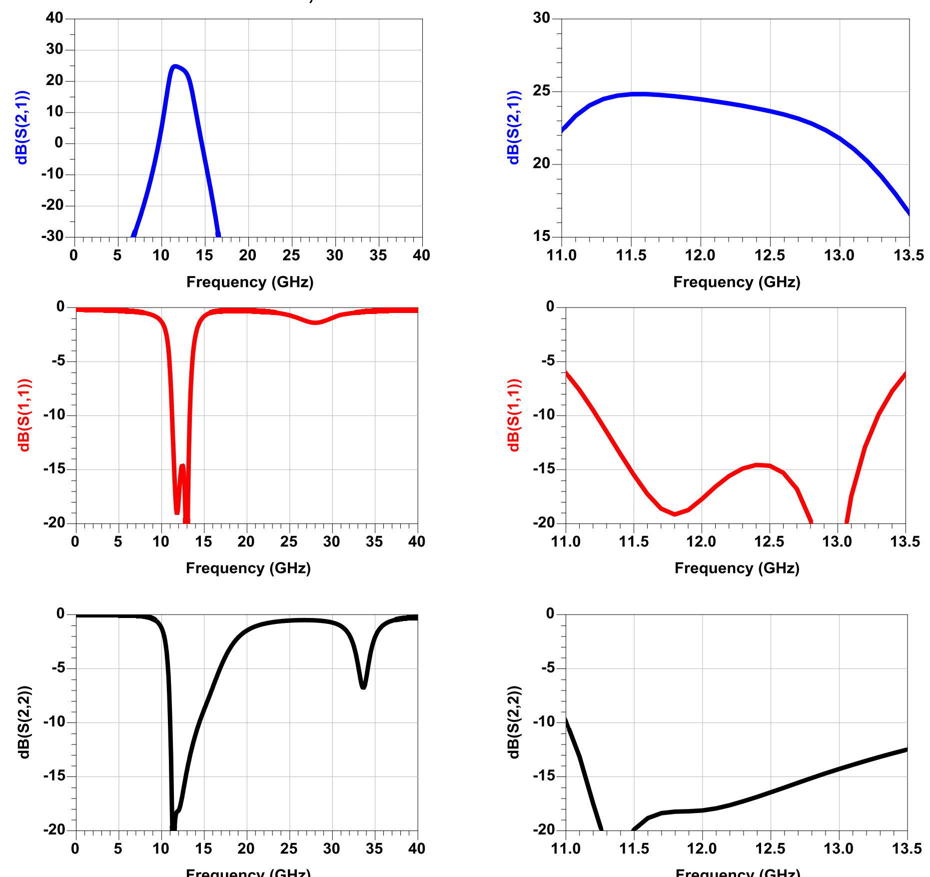

Figure 185 : S-parameters simulation (S21, S11, S22) at room temperature

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Non-linear simulations have been performed with the following setup :

- Input power : -10 to 28dBm (with narrow 0.5dB input power step from 23 to 28dBm)
- Frequency bandwidth : 11 GHz to 13.5 GHz step 0.25GHz

Main RF power performances are:

Figure 186 : HPA-2 module. Simulation results. Output power, power gain and PAE performances

The PAE performances don't match the required performances with a peak PAE of 38% at 12.25GHz. Within the frequency bandwidth the minimum power added efficiency is 37%. The output power performances match the required specifications. Maximum output power is 44.62dBm (29W). Regarding the gain performance at compression level, 15dB is reached for the peak PAE which is under the 16dB required in the specifications table.

PAE by transistor for each stage versus input power is given below:

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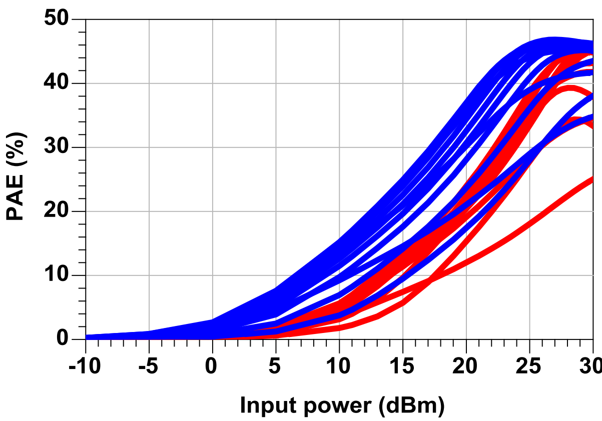

Figure 187 : PAE of stage 1 & 2 versus input power

As expected, the HPA peak PAE corresponds to a maximum peak PAE of stage 2 (46%) close to the maximum PAE found in load pull simulation at 12.25GHz (58%) in the overall frequency bandwidth. The PAE overall HPA power added efficiency remains constant close to 46% in the frame of 11.5 GHz to 13GHz .
The load cycles of the transistors of each stage at biasing point condition equal to IDS0=50mA/mm and VDS=28V , at PIN=28 dBm and several frequencies are shown in Figure 18.
The load cycle for all frequencies, all input power are drawn in red . The remarkable load cycle in blue corresponds to the 12.25GHz (center frequency) for the peak PAE at 28dBm. Load-cycles are correlated to the theoretical optimum PAE shape.

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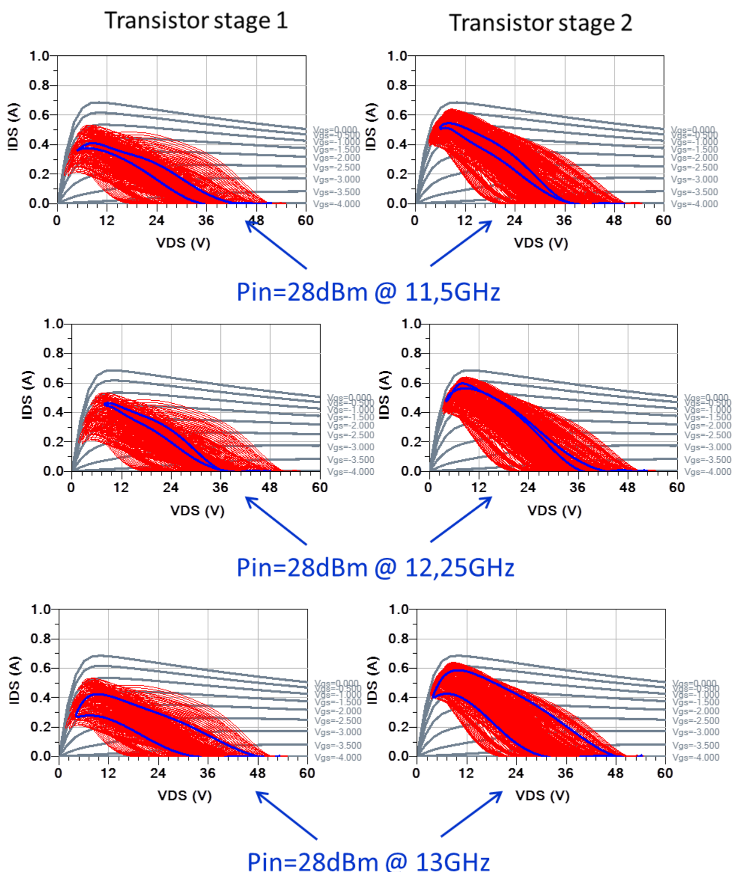

Figure 188 : Transistor load-cycle at 11.5GHz, 12.25GHz and 13GHz (Pin = 28dBm), stage 1 & 2

DC Power Consumption of HPA-2 module is presented below:

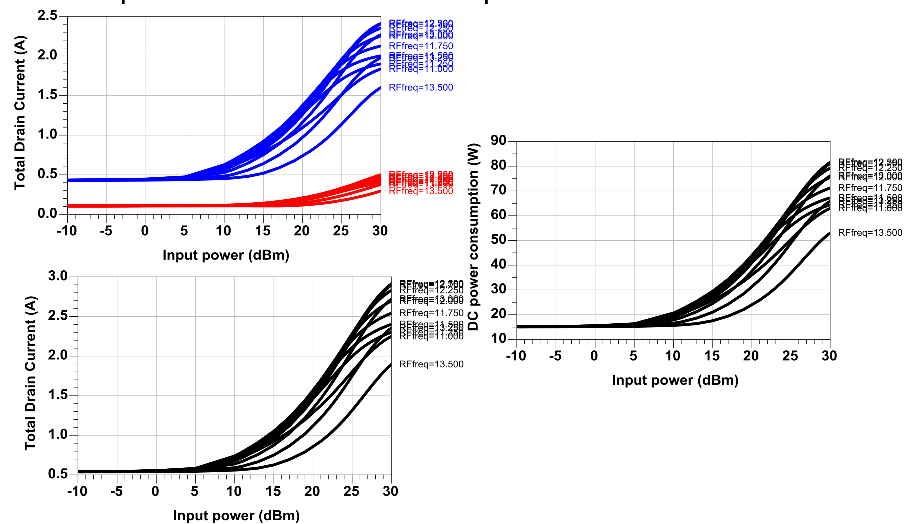

Figure 189 : DC current and power consumption

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Stability analysis has been consolidated by STAN software simulations during linear and non-linear operating modes at baseplate temperature equal to -10 °C.
No critical behavior detected in linear simulation with the following biasing conditions:

- Fixed Ids=50 mA/mm and sweep of Vds from 0V to 30V (step 5V)
- Fixed Vds=28V and sweep of Vgs from -4V to -3V (step 0.1V)

No critical behavior detected in non-linear simulation at biasing condition (equal to 50mA/mm of drain current and Vds=28V) and with a sweep of input power from -10 dBm to 30 dBm. This analysis has been performed in the broadband frequency between 11.5 GHz and 13 GHz.

3.5.2 Detailed Design of version 2: MMIC Doherty HPA module

For this design, elementary building blocks from previous HPA-2 module have been used. Thus, two half HPA-2 modules have been used:

- One half HPA-2 module is used for carrier path
- One half HPA-2 module is used for peaking path

The 2 amplifiers (peaking and carrier) have the same gate length of 4 * 8 * 125um ie 4 mm for last stage. For the input coupler, a Lange coupler which has 90 ° of phase shift over a wide frequency band has been used. For output coupler, solution used is based on the outputs of the following publication « Designing an Octave-Bandwidth doherty amplifier using a novel power combination method N. Sahan and S. Demir Progress In Electromagnetics Research B, Vol. 56, 327-346, 2013 »

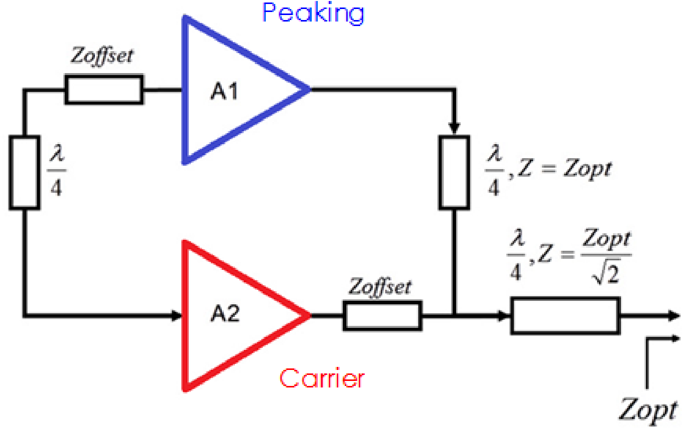

Figure 190 : Doherty MMIC HPA module. Topology

The design methodology has followed the sequence presented below:

1. Use of 2x 10W amplifier cells from HPA-2 module as basic building blocks: the HPA-2 module is divided in two identical and separated parts. Then
    a. One part has been optimized as ‘’peaking’’ amplifier
    b. Second part has been optimized as ‘’carrier’’ amplifier

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2. Use of an ideal 90° coupler input/output and tuning of the VGs _peaking value in order to optimize the operating are of the peaking amplifier vs carrier amplifier)
3. Optimization of the output coupler in order to obtain the bandwidth, the minimum of losses and the required phase shift
4. Optimization in harmonic balance of the input coupler and the inter-stages (of peaking amplifier and carrier amplifier) at Pin=19 dBm (5dB OBO) and Pin=29 dBm (0dB OBO)

Figure 191 : Doherty MMIC HPA module. MMIC circuit layout

Carrier and peaking transistor loadpull simulations are presented in the two following figures:

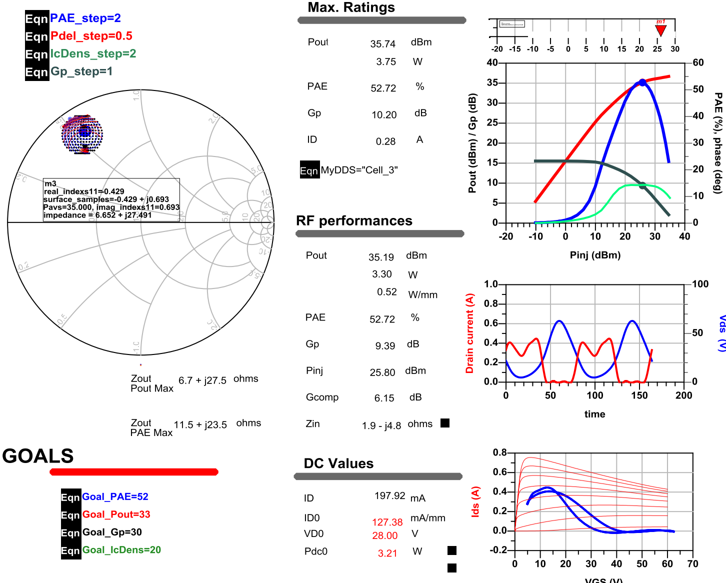

Figure 192 : Load pull 8x125um @12.2GHz @130mA/mm as Carrier transistor

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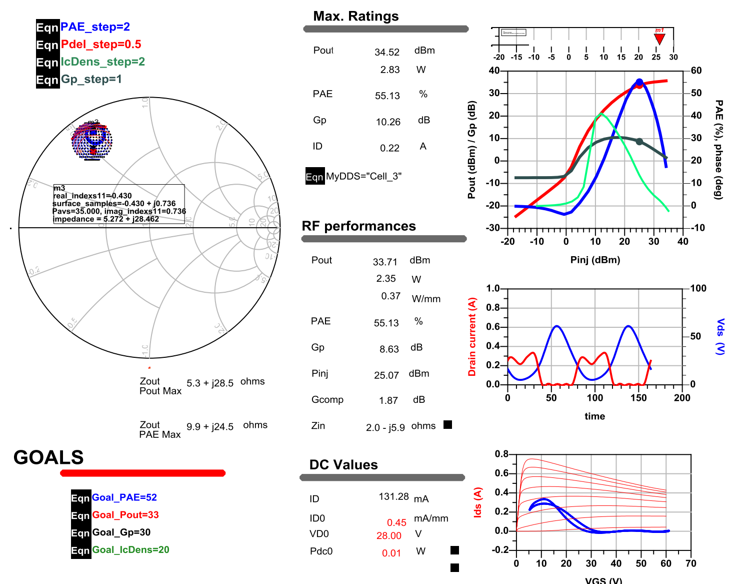

Figure 193 : Load pull @12.2GHz @0mA/mm as peaking transistor

Vg1 of peaking amplifier is optimised to have K>1, it has very low impact on PAE at low signal. The behaviour of the gain is improved as the RF power rise a sufficient value to polarized the peaking amplifier. Due to the large bandwidth of the output coupler and for some cases with low power and RFfreq=[11.5GHz-13GHz], it is observed that some energy produced by the carrier amplifier is absorbed by the peaking amplifier. This behaviour disappears during the increasing of gain of the peaking amplifier.

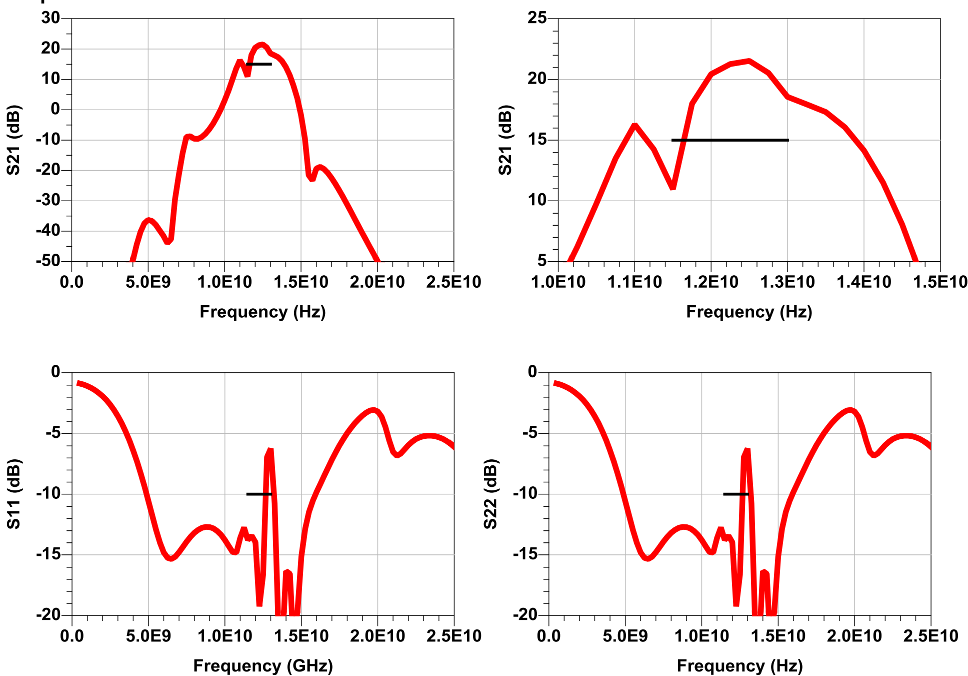

Figure 194 : S Parameters simulation of MMIC Doherty HPA module

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Comparison between Doherty and a classical 20W HPA regarding PAE parameter is provide below:

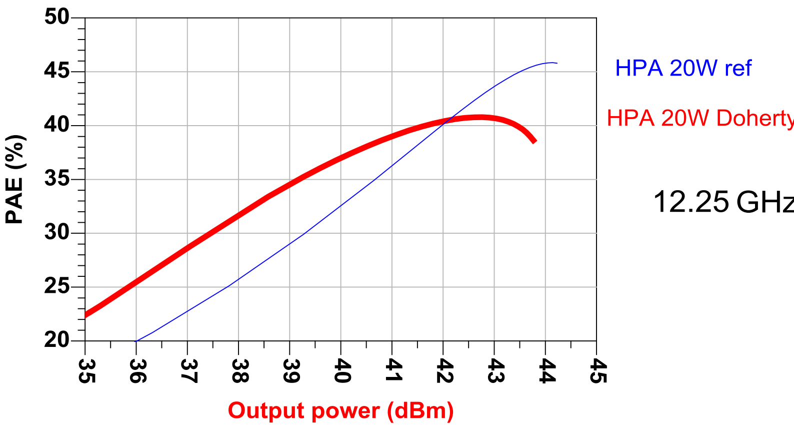

Figure 195 : Comparison between Doherty and a classical 20W HPA regarding PAE parameter

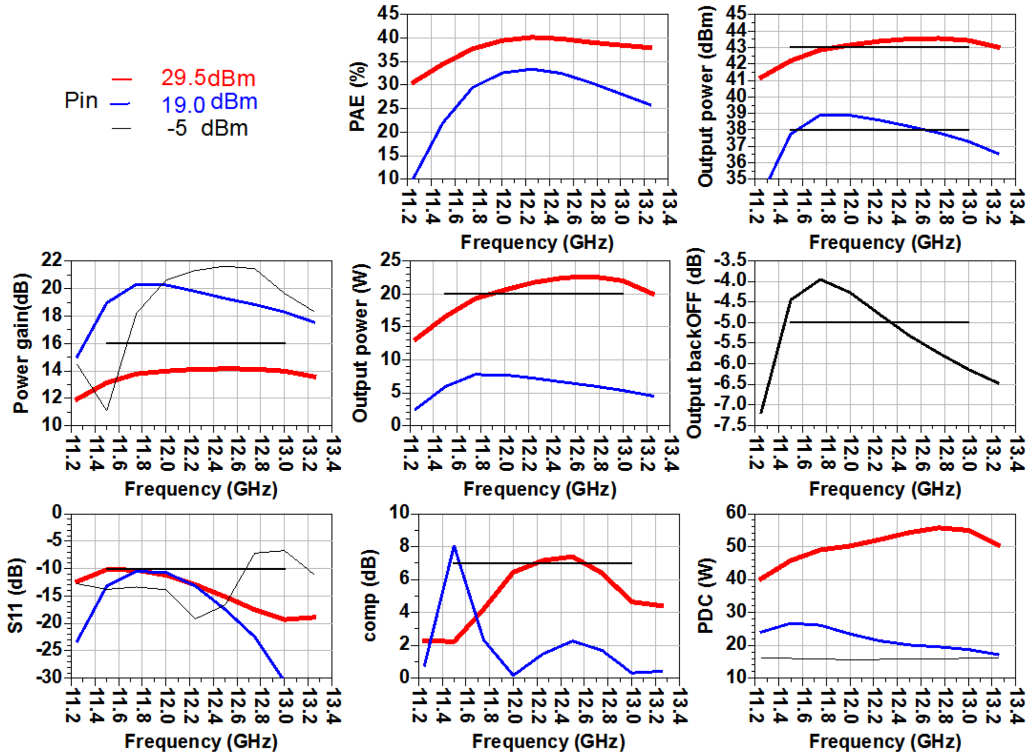

Figure 196 : MMIC Doherty HPA module. Performance over frequency for two different input power

Hereafter are presented the impedances presented at the transistor of both amplifier (carrier and peaking) in function of input power and for each frequency. In low signal, the impedance is outside the smith chart for the peaking amplifier (it means it is off, there no amplification). Moreover, the impedance on the carrier amplifier is also a function of the input power

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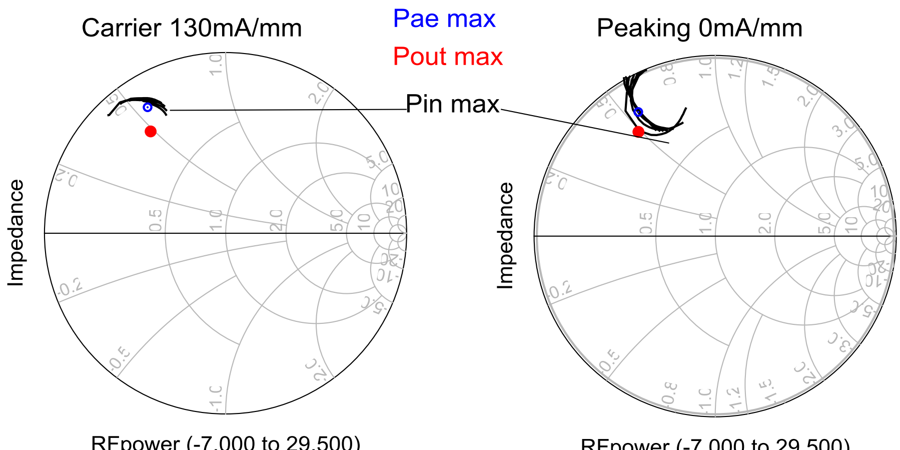

Figure 197 : 2nd stage Transistor Load Pin -7 to 29.5dBm Freq 11.5 to 13 GHz

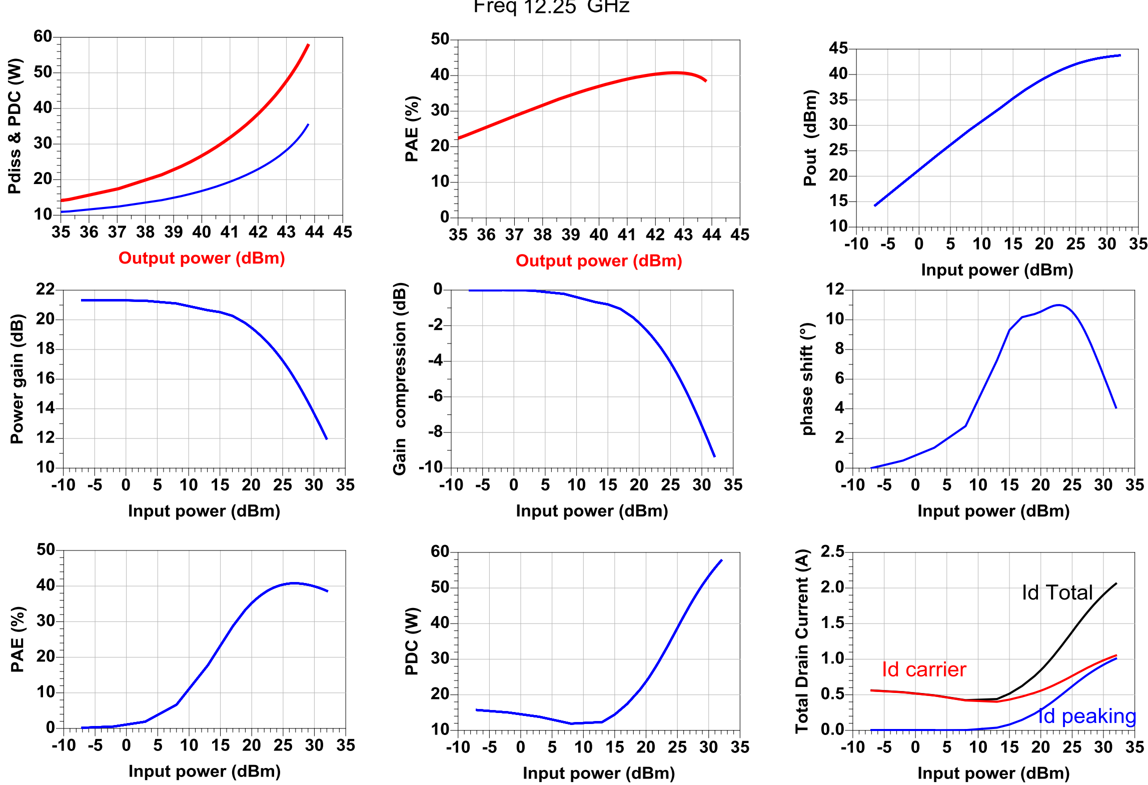

Figure 198 : MMIC Doherty HPA module. NL simulation versus Pin at 12.25 GHz

By tuning the vg peaking value a trade-off between maximum output power and PAE in back-off can be obtained:

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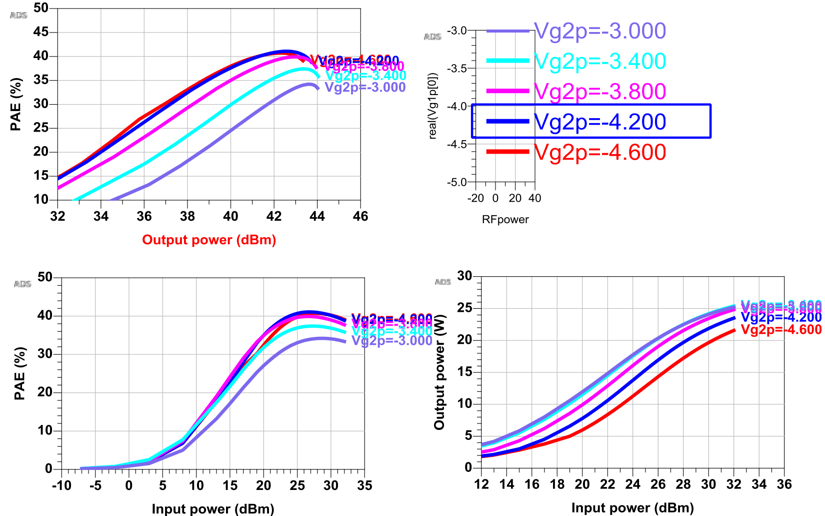

Figure 199 : MMIC Doherty HPA module. Performance versus VG peaking

Stability analysis is consolidated by STAN software simulations during linear and non-linear operating modes at baseplate temperature equal to -20 °C.
No critical behaviour detected in linear simulation with the following biasing conditions:
Probe on Drain and Gate of peaking and carrier amplifier

- Fixed Vgs = -2.95V on Carrier and -4.2V on peaking
- Sweep of Vds from 0V to 30V (1 to 10V step 1V 10 to 30V step 5V)
- Sweep frequency 0.1 to 20GHz

3.5.3 Detailed Design of version 3: MMIC-Hybrid Doherty HPA module

For this third version, a dedicated MMIC test pattern is used. Starting from MMIC Doherty HPA version (version 2), the input and output combiners have been suppressed from MMIC. Thus, this dedicated MMIC test cell is including to separated amplifiers (1x carrier amplifier and 1x peaking amplifier)
To build the MMC-Hybrid Doherty HPA module:

- 1x MMIC test cells is used
- The input combiner (Lange coupler) is processed and alumina circuit
- The output combiner is processed and alumina circuit

Tuning possibilities will be performed on alumina circuit.

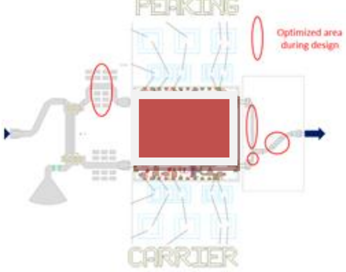

Figure 200 : MMIC-Hybrid Doherty HPA module. Configuration using two MMIC test cells.

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The design methodology has followed the methodology presented below:

1. Load pull simulation on carrier and peaking amplifier. Simulations have been performed for different frequencies in the targeted bandwidth.
2. Design (through EM Simulation) of a an input 90° divider: a Lange coupler topology has been selected and designed.
3. Optimization in harmonic balance of the input offset and of the output coupler offset at Pin=19 dBm (5dB OBO) and Pin=29 dBm (0dB OBO)
4. Global NL simulation of the hybrid Doherty Ku-band amplifier and cross-check that the hybrid output combiner presents the optimum loads to the carrier amplifier and to the peaking amplifier (vs OBO)

The carrier amplifier loadpull simulation is presented in the following figure. We can observe that optimum load to present to the carrier amplifier at nominal operating point (Pae_max) is close to 50ohms: 57-13.1*j ohms.

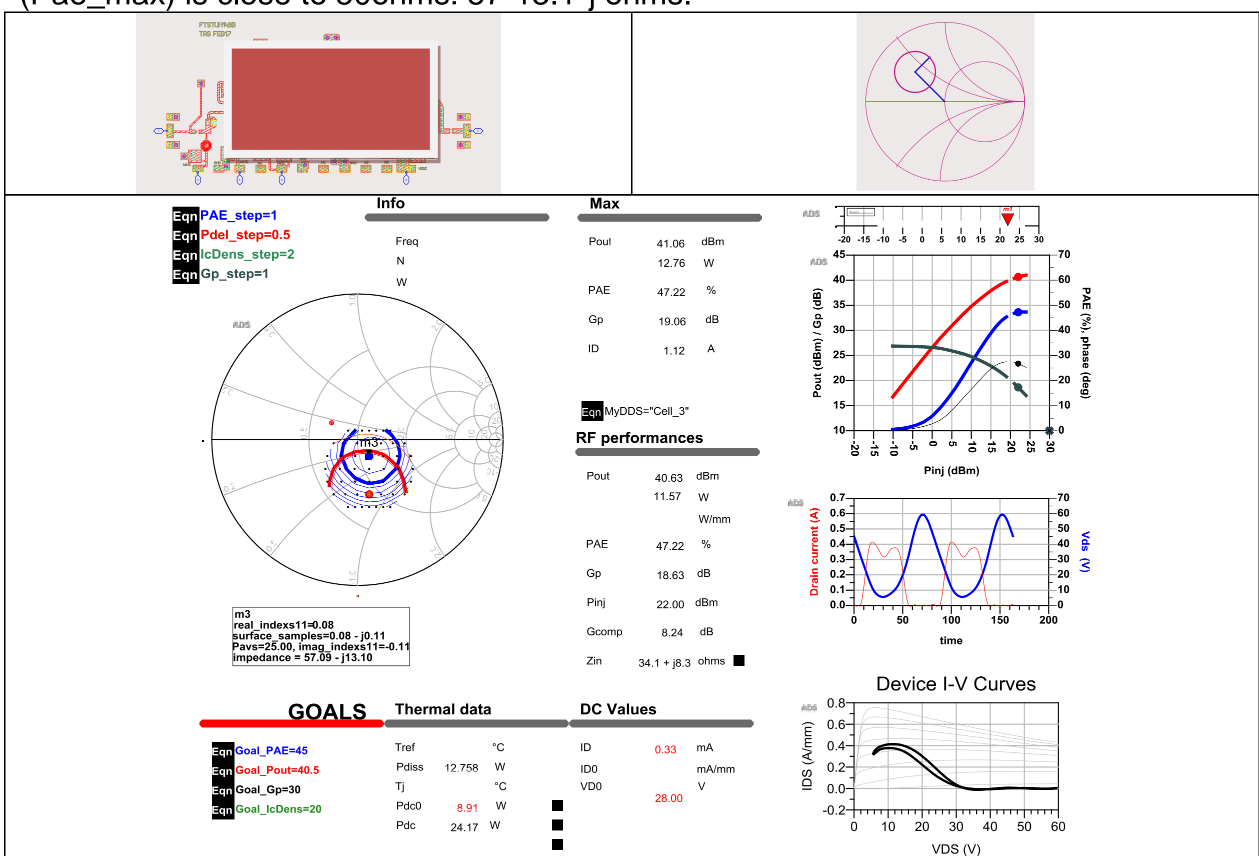

Figure 201 : Load pull simulation and carrier amplifier

The peaking amplifier loadpull simulation is presented in the following figure. We can observe that optimum load to present to the peaking amplifier at Pae_max is equal to 16.6+7.9*j ohms.

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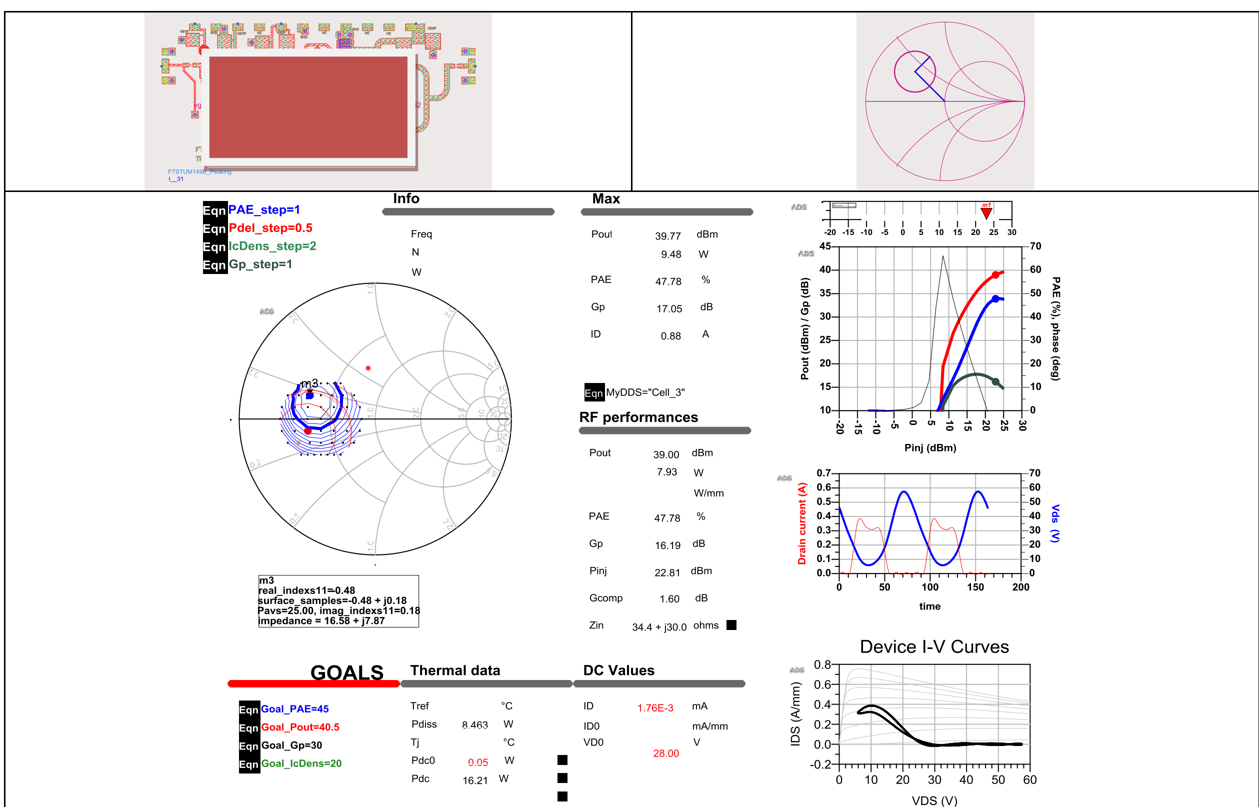

Figure 202 : Load pull simulation and peaking amplifier

Vg1 of peaking amplifier has been optimized in order to have K>1: it has very low impact on PAE at low signal. The behavior of the gain is improved as the RF power rise a sufficient value to polarized the peaking amplifier. Due to the large bandwidth of the output coupler and for some cases (low power and some frequency points into [11.5GHz-13GHz]), it is observed that some level of RF energy produced by the carrier amplifier is absorbed by the peaking amplifier. This behavior disappears during the increasing of gain of the peaking amplifier.

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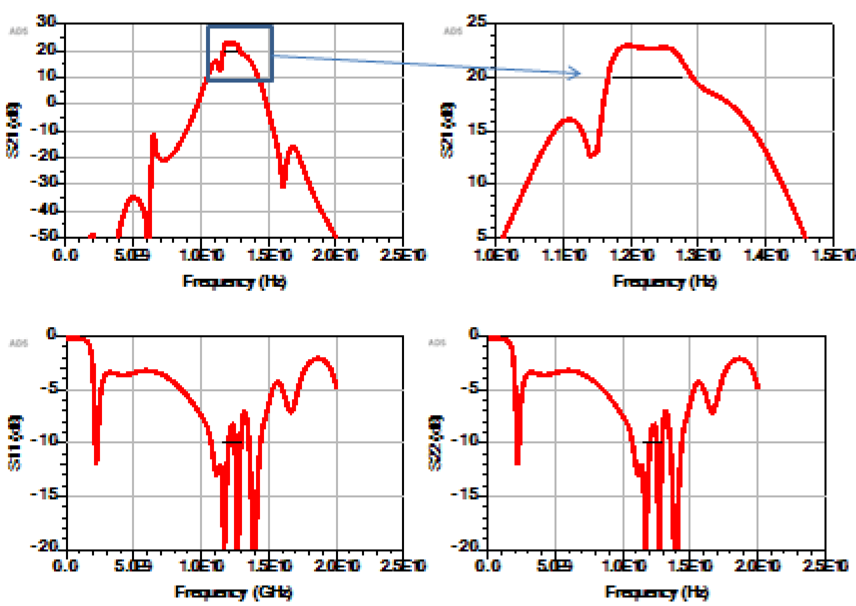

Figure 203 : S Parameters simulation of MMIC-Hybrid Doherty HPA

Comparison between MMIC Doherty / MMIC-Hybrid Doherty and a classical 20W HPA regarding PAE parameter is provide below:

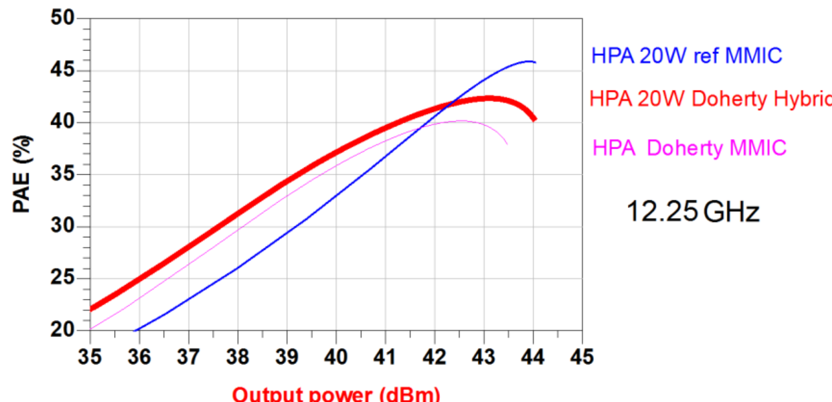

Figure 204 : Comparison between Doherty and a classical 20W HPA regarding PAE parameter

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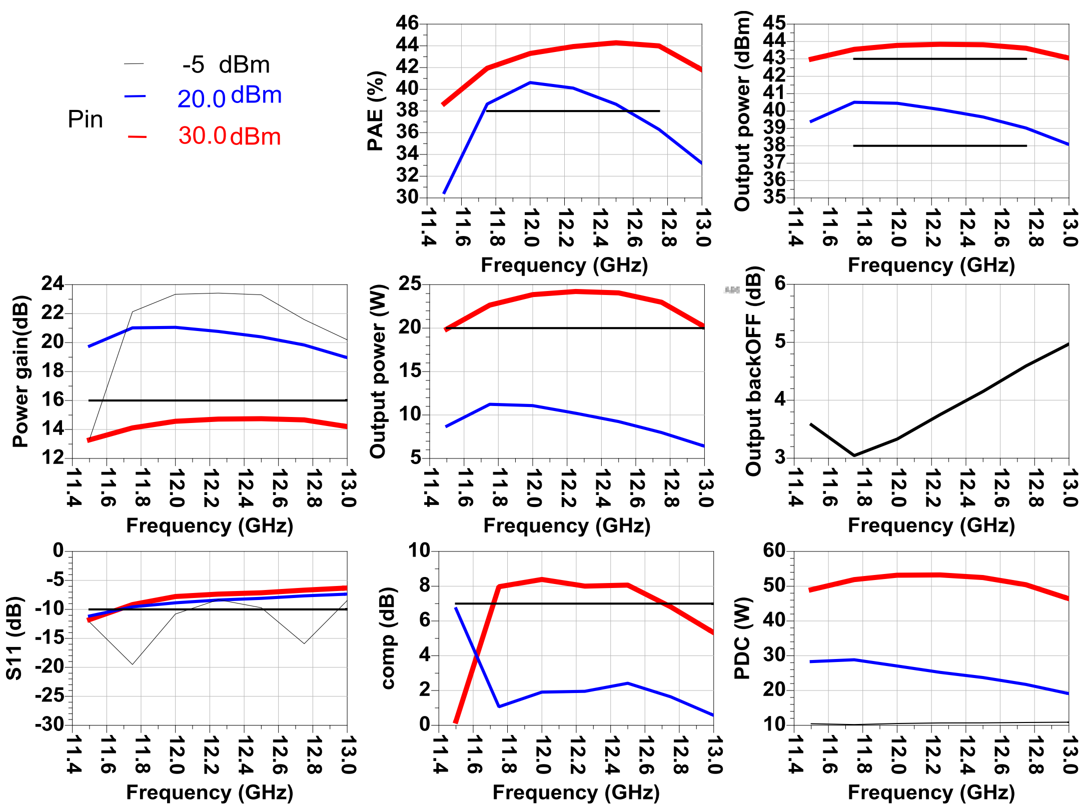

Figure 205 : MMIC-Hybrid Doherty HPA module. Performance over frequency for different input power

Hereafter are presented the impedances presented at the 2nd stage transistors of both amplifier in function of input power and for each frequency. In low signal, the impedance is outside the smith chart for the peaking amplifier (it means it is off, there no gain amplification). Moreover, the impedance on the carrier amplifier is also a function of the input power

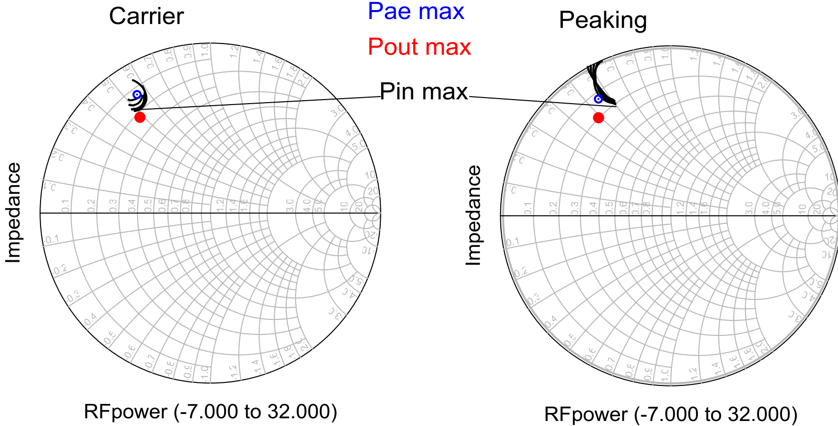

Figure 206 : MMIC-Hybrid Doherty HPA module. 2nd stage Transistor output load for Pin=[-7 to 30dBm]. Freq=[11.5 to 13 GHz]

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Hereafter are presented the impedances presented at the both amplifier in function of input power and for one frequency. In low signal, the impedance is outside the smith chart for the peaking amplifier (it means it is off, there no amplification).

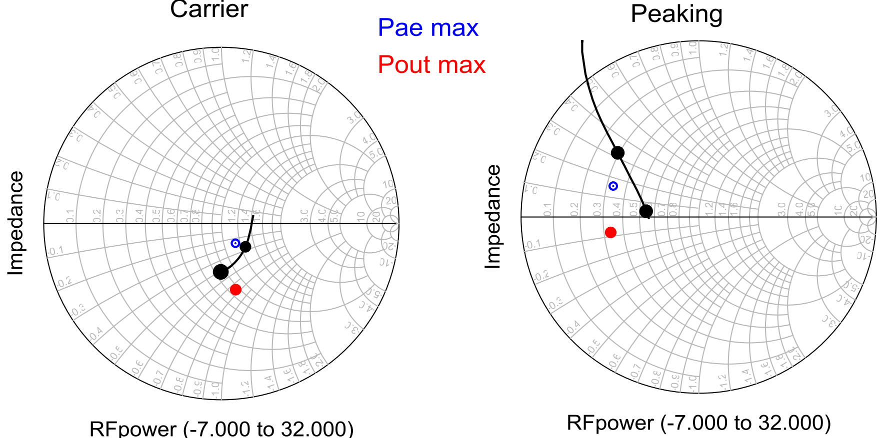

Figure 207 : MMIC-Hybrid Doherty HPA module. Amplifier (Carrier & Peaking) loads for Pin=[-7 to 30dBm]. Freq 12.25 GHz

Three types of Ku-Band HPA module using UMS GH25 technology have been designed. Objective of the manufacturing and tests is to identify solution to achieve best trade-off for Pout/PAE/NPR/bandwidth performance.

3.6 0,25µm MMIC and transistors Manufacturing and on-wafer Test

A complete GH25 wafer (Run ''Wind'') including the different MMICs designed and presented in the previous chapter has been manufactured by UMS at Ulm facilities. On-wafer tests have been conducted by UMS ar Villebon facilities:

- Process monitoring
- On-wafer DC&RF tests of the transistor cells and the different MMIC

3.6.1 PCM Results

PCMs results are presented in the table below. These PCM results demonstrate very low spread on the WIND wafer on both active and passive devices.

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I3 - R_sheet_ZA Measurement: F @ 06.06.2017 F124517 - WIND_001 Target: 495 Spec: (U: 525 - L: 465) Warn: (U: 520 - L: 470)	I3 - IDS+__V1Sdc Measurement: F @ 06.06.2017 F124517 - WIND_001 Target: 1000 Spec: (U: 1100 - L: 900) Warn: (U: 1075 - L: 925)	I3 - Vg100_V1Sdc Measurement: F @ 06.06.2017 F124517 - WIND_001 Target: -3.45 Spec: (U: -2.80 - L: -4.00) Warn: (U: -3.00 - L: -3.80)
Sheet resistance of the active area	Saturated drain current at Vgs=+1V	Pinch-off voltage at drain current= Idss/100
I3 - IdIHV_V1Sdc Measurement: F @ 06.06.2017 F124517 - WIND_001 Target: 20.00 Warn: (U: 150.00 - L: 1.00)	I3 - R_RM_6_2 Measurement: F @ 06.06.2017 F124517 - WIND_001 Target: 30.0 Spec: (U: 34.0 - L: 26.0) Warn: (U: 33.0 - L: 27.0)	I3 - C_Capa Measurement: F @ 06.06.2017 F124517 - WIND_001 Target: 255 Spec: (U: 275 - L: 235) Warn: (U: 270 - L: 240)
Drain current leakage under high drain voltage	TaN sheet resistor	MIM Capacitor

Figure 208 : PCM results of GH25 wafer

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3.6.2 HPA-2 MMIC On wafer-measurements

The test conditions are reminder below:

Pulsed S-Parameters measurement:	Power pulsed measurement:
• Vd 28V Pulsed Vg 25µs / 10%, Idq=50mA/mm • From 0.5 to 20 GHz (step 0.1 GHz)	• Vd 28V Pulsed Vg 25µs / 10%, Idq=50mA/mm • Freq=[11.5-13GHz] step 0.25 GHz. • Pin 0 to 30 dBm (0 , 10 ,20 to 30 step 1dB) • Record : Pin, Pout, Ig, Id

Table 32 : HPA-2 MMIC On wafer-measurements. Test conditions

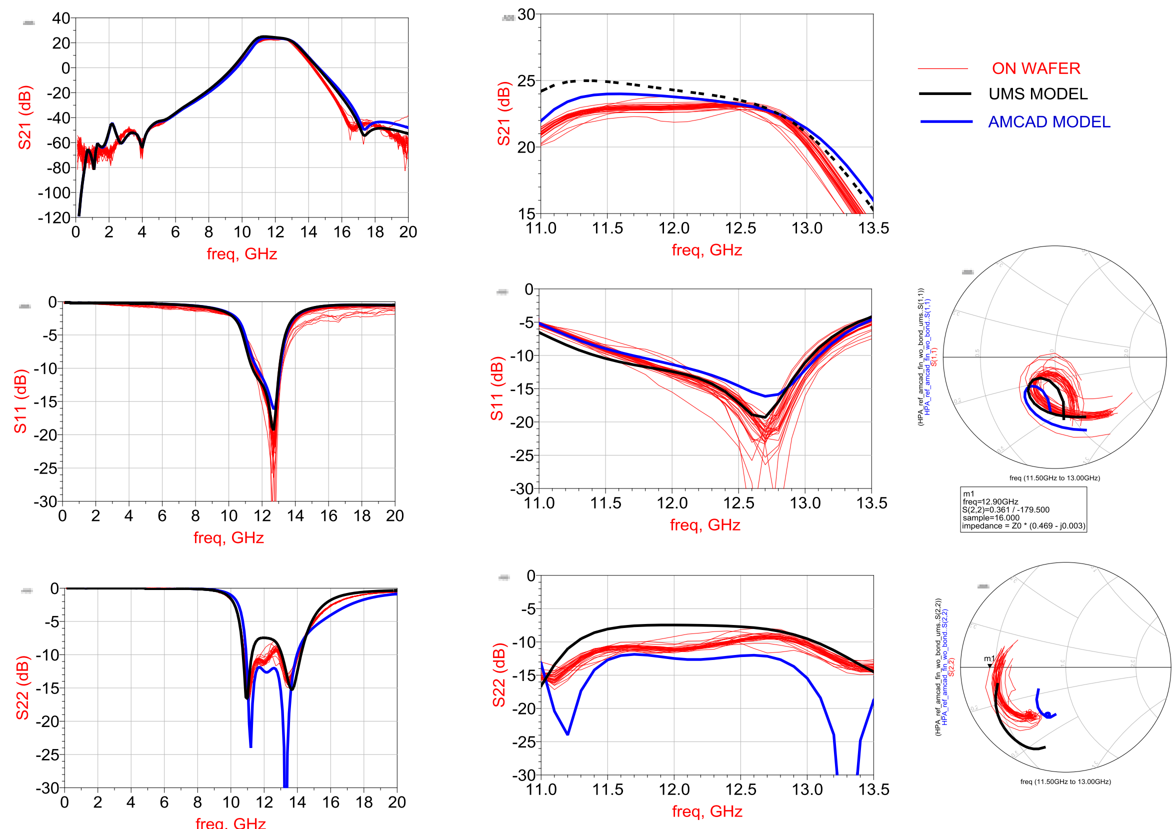

Figure 209 : HPA-2 MMIC On wafer-measurement. [S] Parameter measurements and simulation

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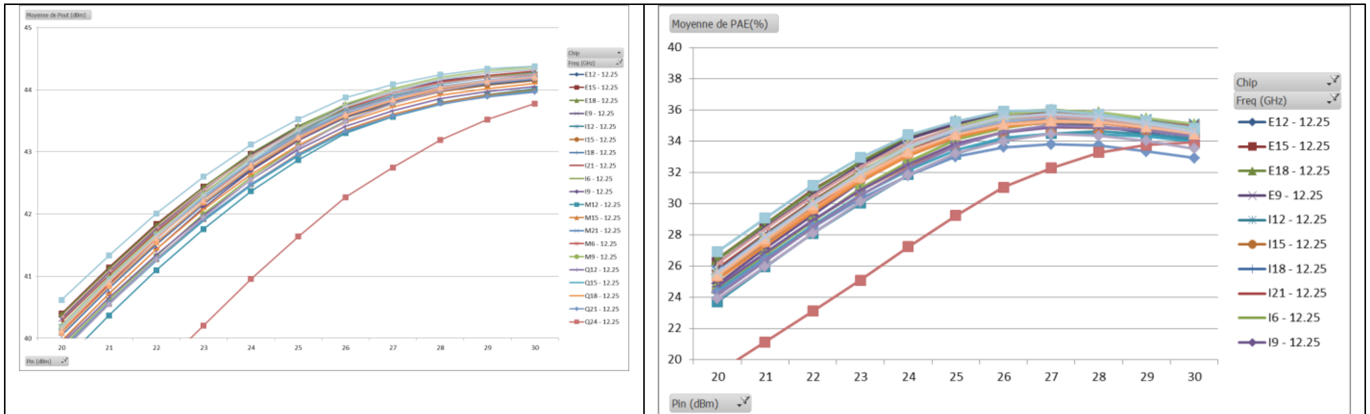

Figure 210 : HPA-2 MMIC On wafer-measurement. Power measurements. Pout and PAE vs Pin at 12,25 GHz

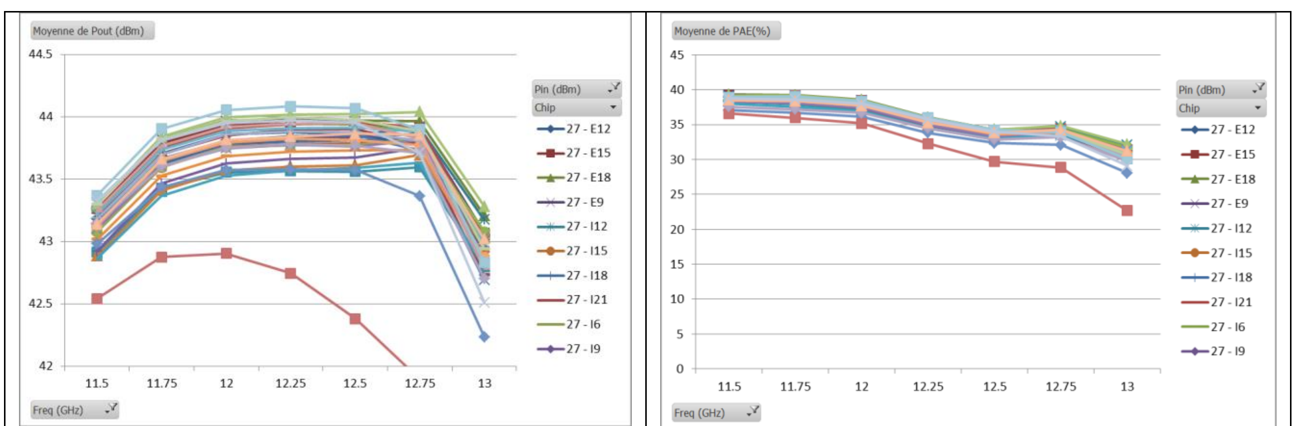

Figure 211: HPA-2 MMIC On wafer-measurement. Power measurements. Pout and PAE vs freq at Pin=27 dBm

3.6.3 Doherty HPA MMIC On wafer-measurements

The test conditions are reminder below:

Pulsed S-Parameters measurement:	Power pulsed measurement:
• Vd 28V Pulsed Vg 25µs / 10%, Idq=50mA/mm • From 0.5 to 20 GHz (step 0.1 GHz)	• Vd 28V Pulsed Vg 25µs / 10%, Idq=50mA/mm • Freq=[11.5-13GHz] step 0.25 GHz. • Pin 0 to 30 dBm (0 , 10 ,20 to 30 step 1dB) • Record : Pin, Pout, Ig, Id

Table 33 : Doherty HPA MMIC On wafer-measurements. Test conditions

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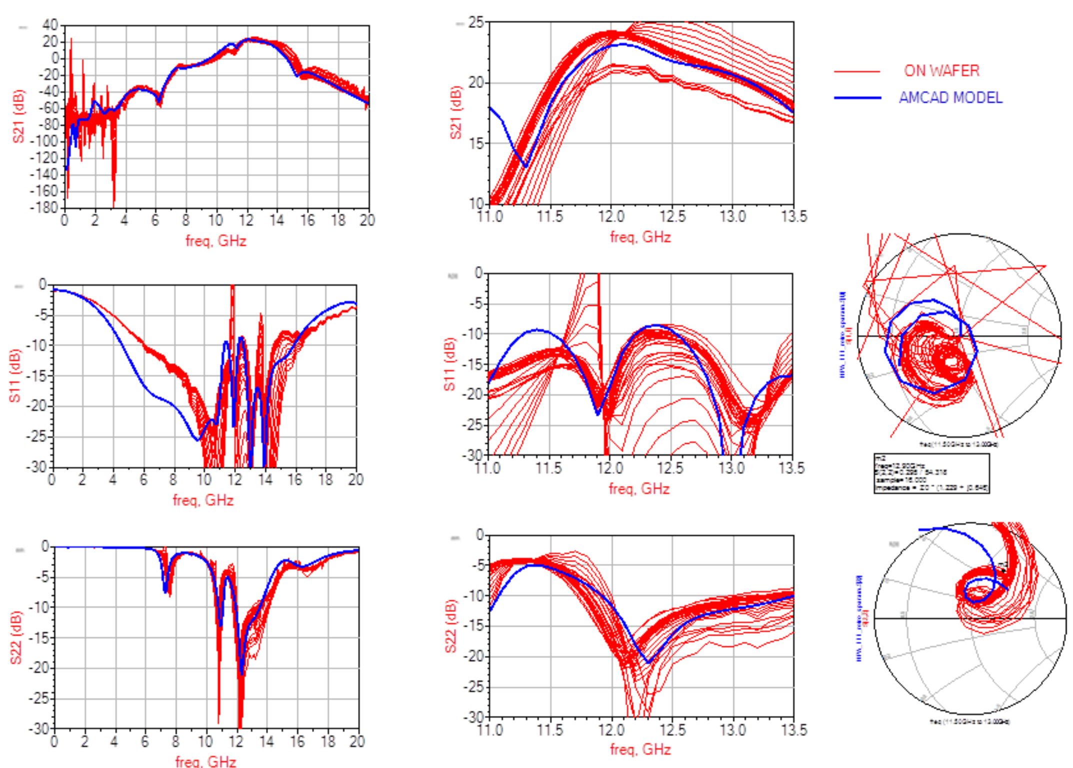

Figure 212 : Doherty HPA MMIC On wafer-measurement. [S] Parameter measurements and simulation

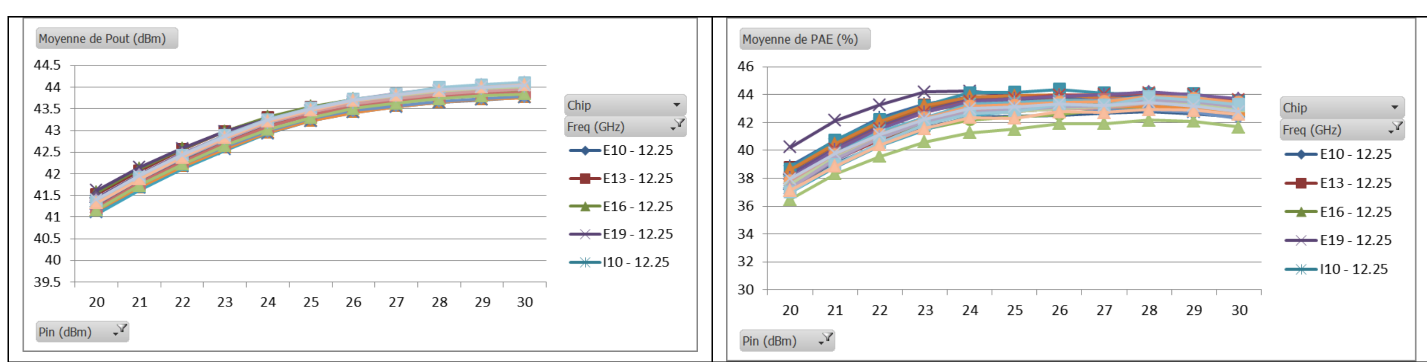

Figure 213 : Doherty HPA MMIC On wafer-measurement. Power measurements. Pout and PAE vs Pin at 12,25 GHz

Some comparison simulations vs measurements are provided in the following figures:

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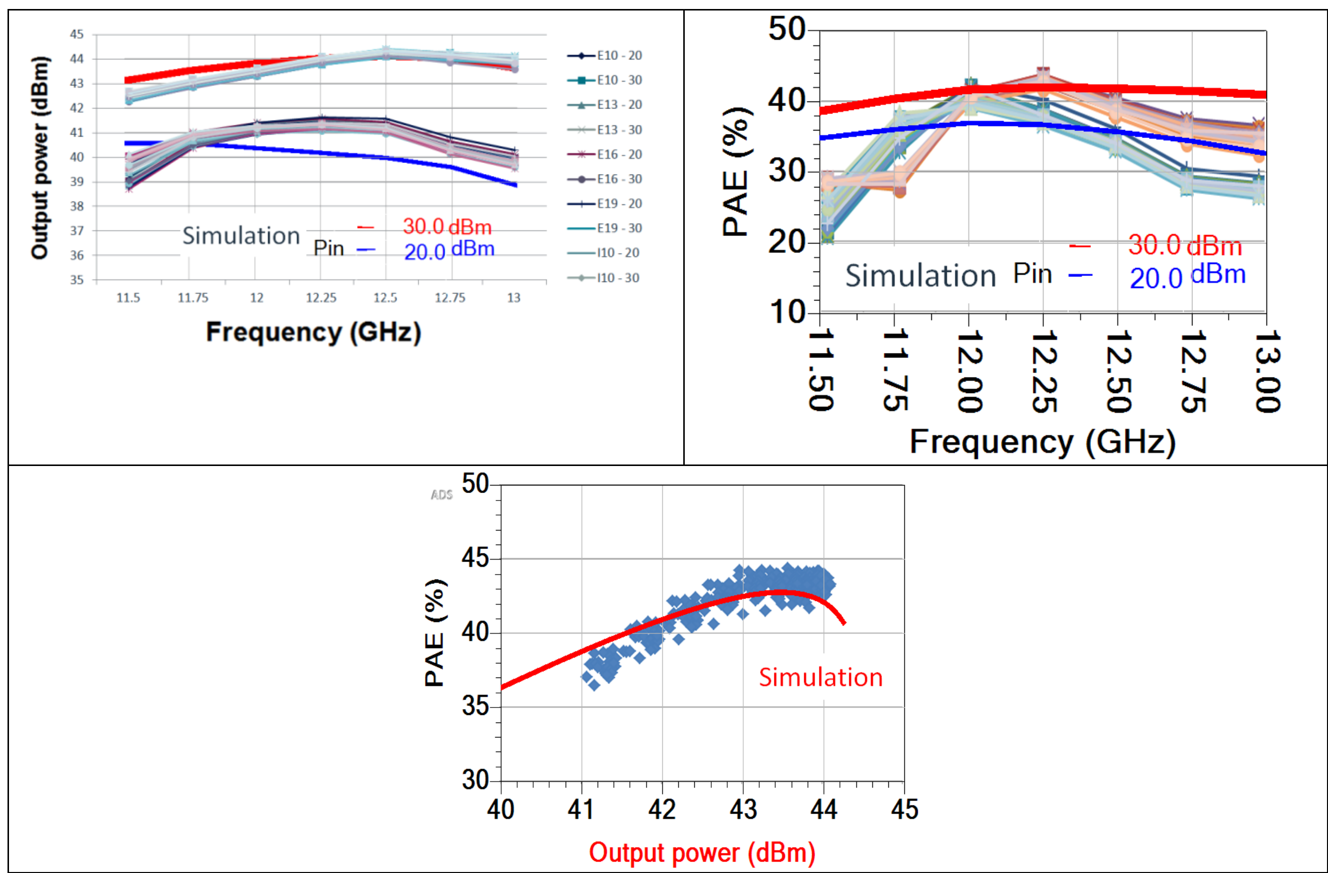

Figure 214 : Doherty HPA MMIC On wafer-measurement. Pout & PAE vs freq Measurements and simulation at Pin=20&30 dBm

3.7 HPA-2 Module and Doherty HPA Module Test

The manufacturing and testing activities conducted are:

- HPA-2 modules:
    - 4x samples have been mounted in jig test fixture
    - [S] parameter measurements vs temperature
    - CW-mode multi-carrier mode measurements vs temperature
    - RF step measurements at room temperature
- MMIC Doherty HPA modules:
    - 3x samples have been mounted in jig test fixture
    - [S] parameter measurements vs temperature
    - CW-mode multi-carrier mode measurements vs temperature
- MMIC-Hybrid Doherty HPA modules:
    - 2x samples have been mounted in jig test fixture
    - [S] parameter measurements vs temperature
    - CW-mode mode measurements at room temperature

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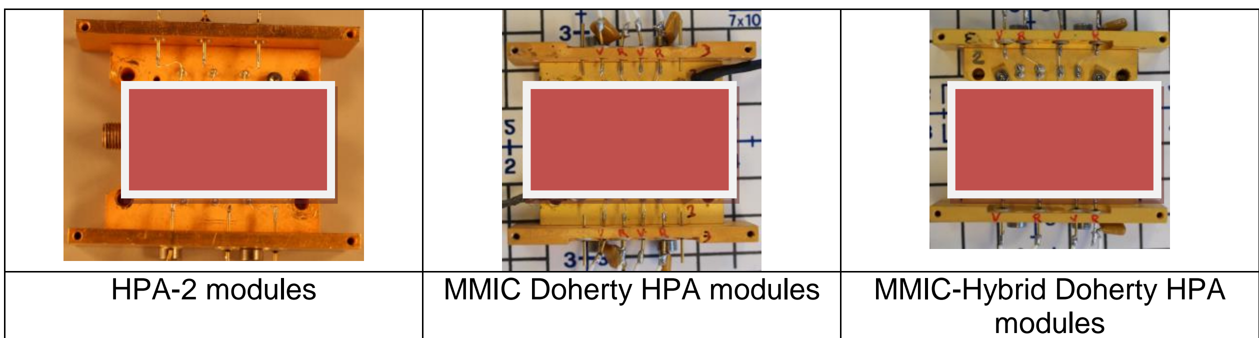

HPA-2 modules	MMIC Doherty HPA modules	MMIC-Hybrid Doherty HPA modules

Figure 215 : Photography of HPA-2 modules and Doherty HPA modules

3.7.1 HPA-2 Modules test results

3x GH25 HPA-2 modules have been tested: in the frame of this study, tuning of the HPA modules has been performed at Temp=25°C with CW signal in order to achieve maximum of PAE. Then [S] parameter measurements and power measurements with multi-carrier signal has been conducted.

The results are presented with the following outline

- [S] parameters measurements versus Temp=[-10°C, 25°C, 85°C]
- Power measurements (CW signal) versus Pin. Temp=[-10°C, 25°C, 85°C]. Vds=40V RF=[11.5 to 13GHz] with RF step=500MHz
- Power measurements (multi-carrier signal) versus Pin. Temp=[-10°C, 25°C, 85°C]. Vds=30V, Ids=450mA at centre frequency = 12 GHz
- RF step stress measurements

3.7.1.1 [S] Parameter measurements.

Hereafter, the HPA-2 #1 module S-parameters are given over a DC to 20GHz bandwidth with drain voltage of 30V and Ids=450mA (45mA/mm) fixed at Temp=25°C. Measurements are performed versus Temp=[-10°C, 25°C, 85°C]

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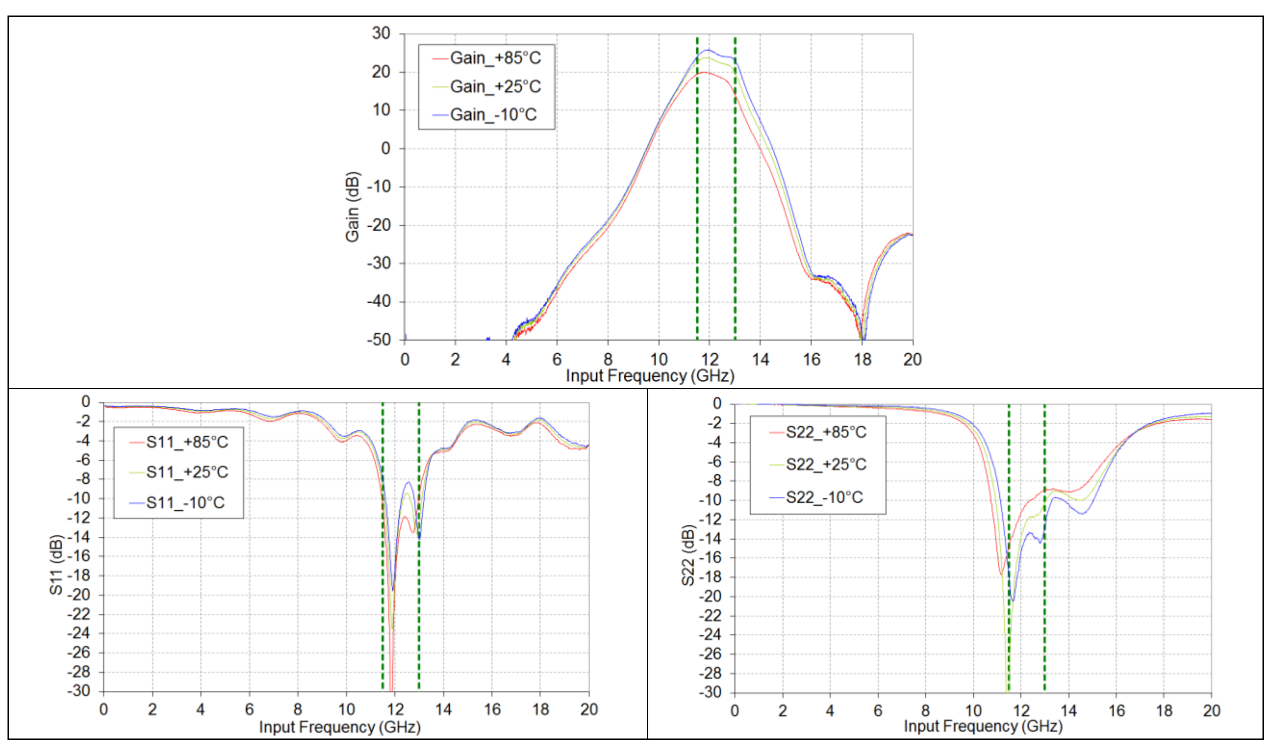
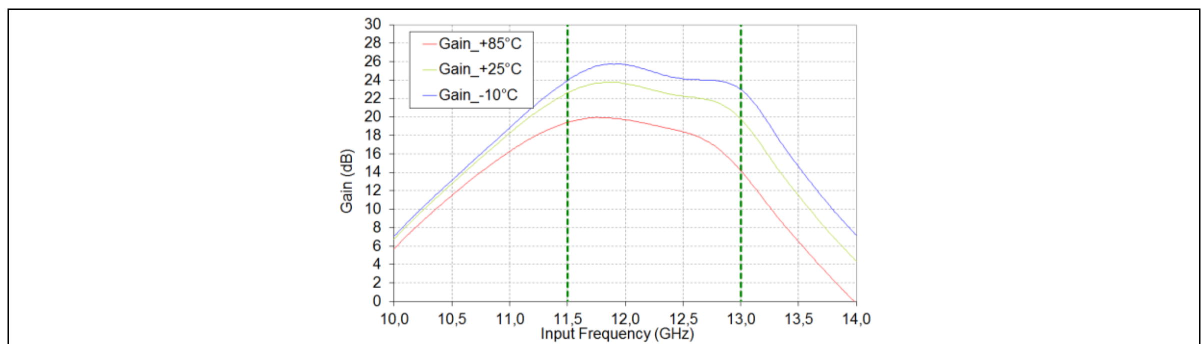


Figure 216 : HPA-2 #1 module. [S] parameters measurements. RF=[DC-20GHz], Vd=30V, Fixed drain current Ids=450mA @25°C, Temp=[-10°C, 25°C, 85°C]

On the following figures, we focus on the HPA-2 #1 module in-band frequency behavior. **Erreur ! Source du renvoi introuvable.** shows that S11 and S22 parameters varies not in the same way:

- Input return loss is optimum at hot temperature
- Output return loss is optimum at room temperature.

S21 variation is about 6dB between -10°C to 85°C at 12 GHz. At constant gate voltage current, the gain variation versus temperature is 0,31dB/°C



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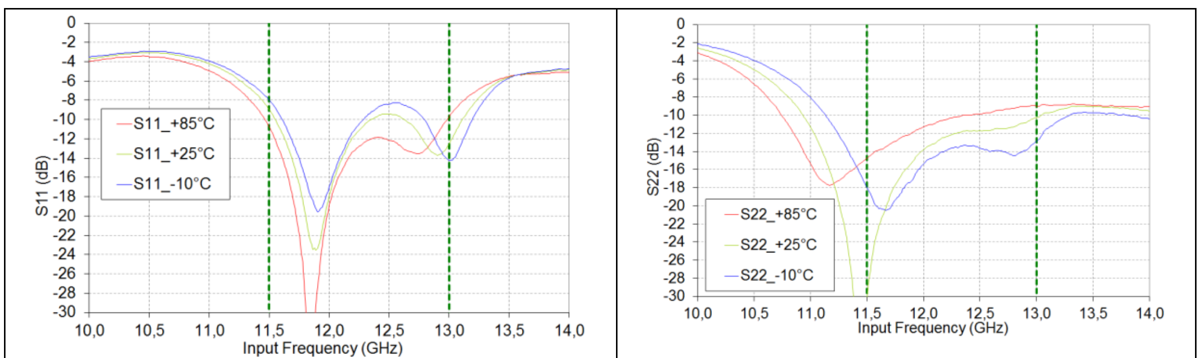

Figure 217 : HPA-2 #1 module. [S] parameters measurements. RF=[10-14GHz], Vd=30V, Fixed drain current Ids=450mA @25°C, Temp=[-10°C, 25°C, 85°C]

Hereafter, for three HPA modules, the S-parameters are given over a DC to 20 GHz bandwidth with drain voltage of 30V and Ids=450mA (25mA/mm) fixed at Temp=25°C. Measurements are performed versus Temp=[-10°C, 25°C, 85°C]

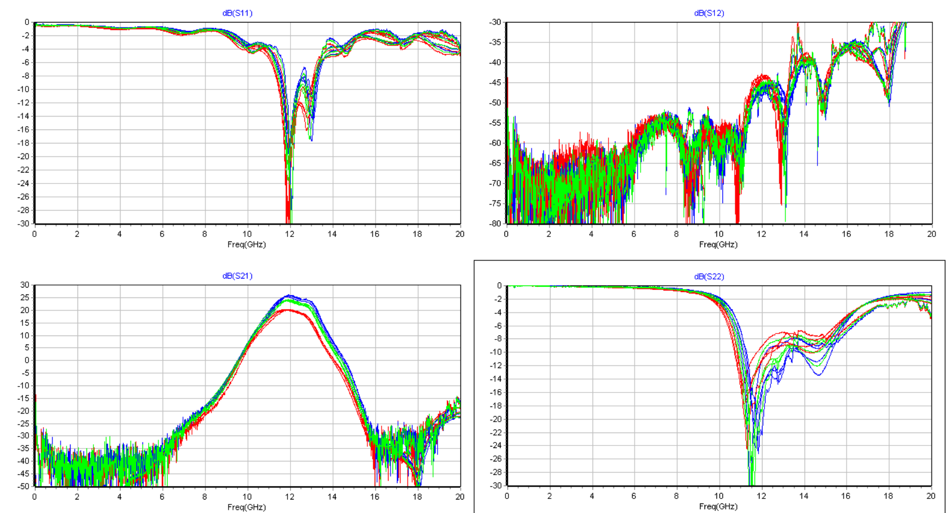

Figure 218 : HPA-2 #1 HPA-2 #2 HPA#" HPA-2 #4 modules. [S] parameters measurements. RF=[DC-20 GHz], Vd=30 V. Fixed drain current Ids=450mA @25°C. Temp=[-10°C, 25°C, 85°C]

On following figures, we focus on the HPA modules in-band frequency behavior. **Erreur ! Source du renvoi introuvable.** shows the dispersion on S11, S22 and S21 parameters versus HPA modules. Measurements are performed versus Temp=[-10°C, 25°C, 85°C]

- Regarding S21 parameter, at 12 GHz, a maximum dispersion of 1dB is observed between the three HPA modules
- Regarding S11 parameter, at 12 GHz, a maximum dispersion of 2dB is observed between the three HPA modules
- Regarding S22 parameter, at 12 GHz, a maximum dispersion of 2dB is observed between the three HPA modules

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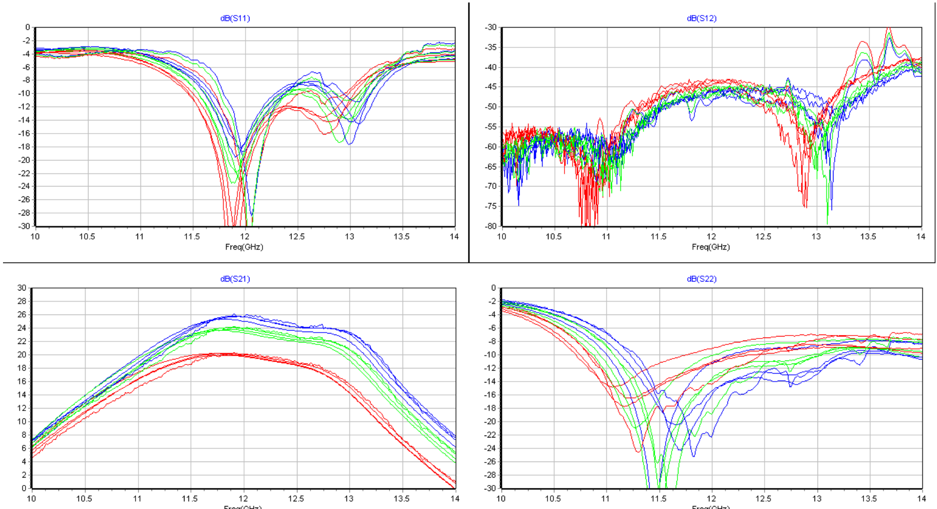
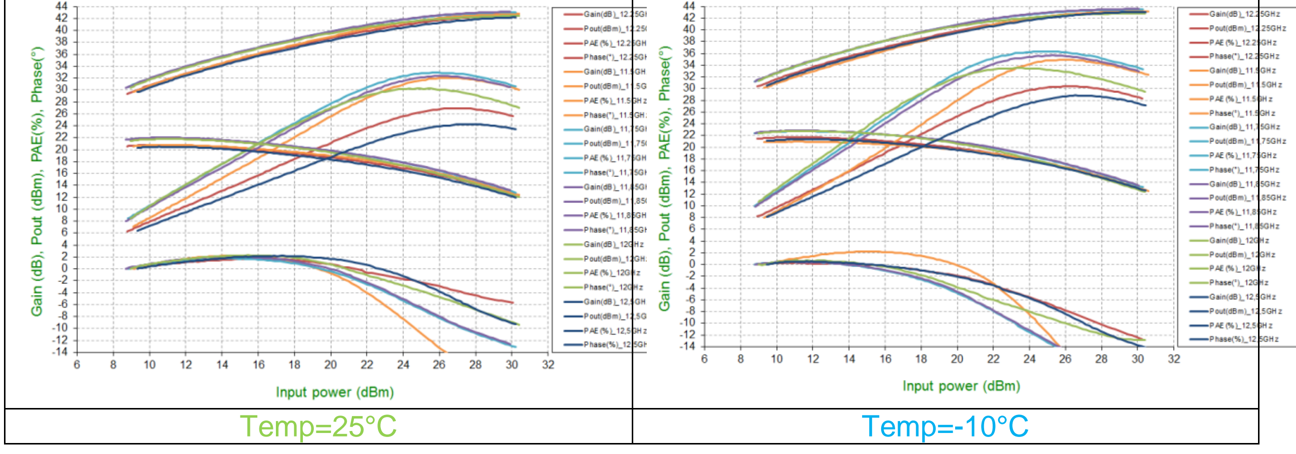


Figure 219 : HPA-2 #1 HPA-2 #2 HPA-2 #3 HPA-2 #4 modules. [S] parameters measurements. RF=[10-14GHz], Vd=30 V, Fixed drain current Ids=450mA @25°C. Temp=[-10°C, 25°C, 85°C].

3.7.1.2 CW mode power measurements.

The main RF performances obtained, output power, PAE, power gain and phase are presented below versus input power and different frequency points from [11.5GHz to 13GHz]. Measurements have been performed for Temp=[-10°C, 25°C, 85°C]. For each frequency, drain current has been tuned in small signal: Ids=450mA (fixed at 25°C) with Vds=30V which represents the best trade-off in term of Pout/PAE/Gain/AMPM.



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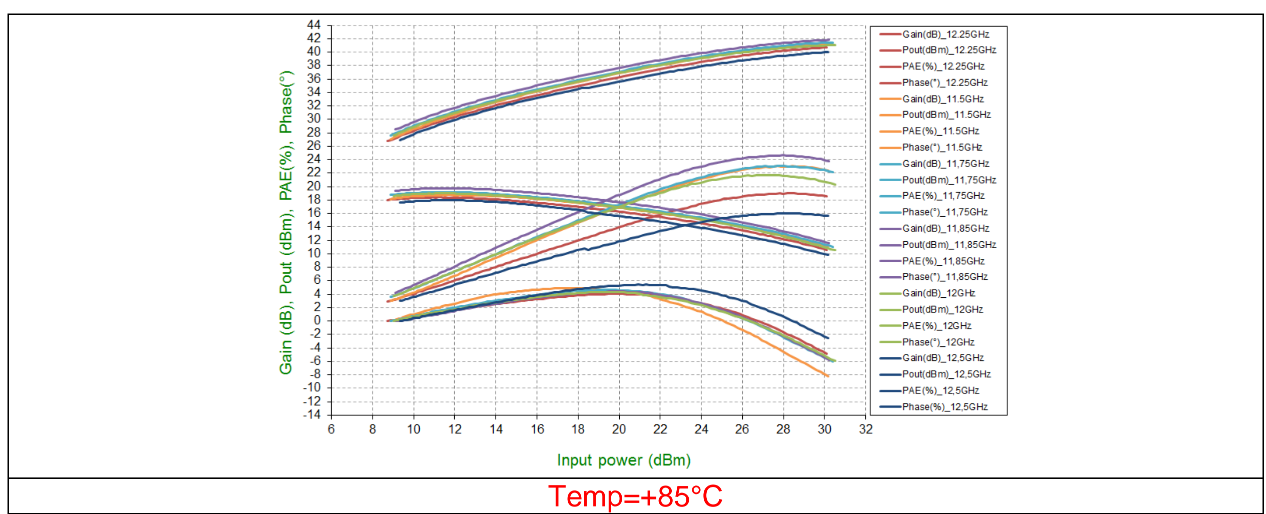

Temp=+85°C

Figure 220: HPA-2 #1 module. Power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vd=30 V, Id=450mA. RF=[11,5 GHz to 13 GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

In figure below, the results (Pout, Gain, PAE, Compression) are presented versus frequency and temperature. For each temperature, Pin has been fixed to obtain maximum of PAE.

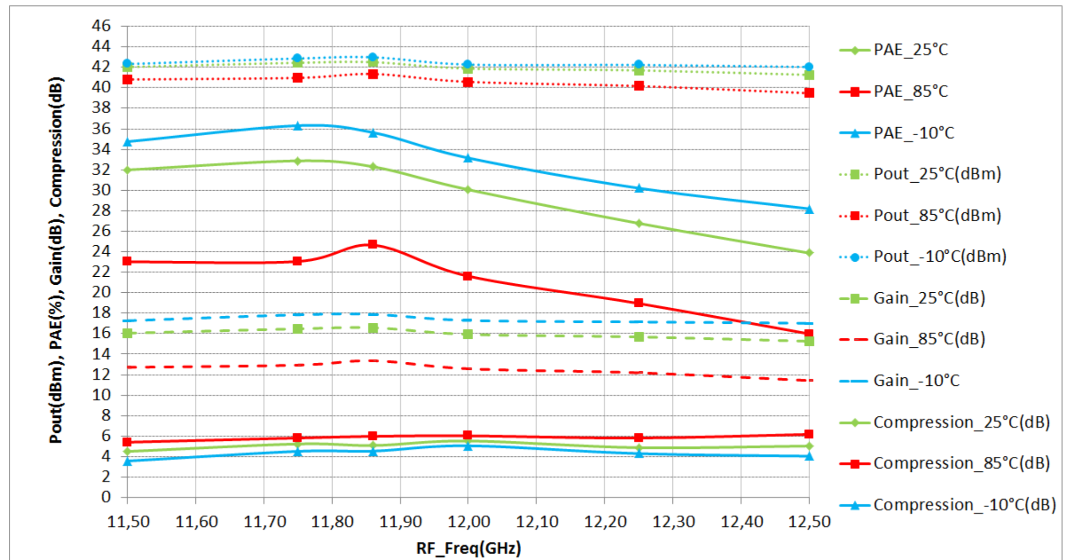

Figure 221 : HPA-2 #1 module. Power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vd=30 V, Id=450mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max.

At Vds=30 V and room temperature, the maximum overall power added efficiency varies from 25 to 32% and is associated to an output power of 14W to 16W. Synthesis of the RF performances measured with CW signal are provided in the following table. Data are provided at PAE_max.

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Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,98	42,04	16,00	16,06	4,51	-13,15	32,00
11,75	25,97	42,45	17,58	16,48	5,24	-8,20	32,88
11,86	25,92	42,51	17,82	16,59	5,09	-7,84	32,31
12,00	25,95	41,89	15,45	15,94	5,53	-4,67	30,07
12,25	26,02	41,71	14,83	15,69	4,88	-2,94	26,78
12,50	26,00	41,27	13,40	15,27	5,04	-3,77	23,88

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	28,10	40,82	12,08	12,72	5,41	-4,74	23,02
11,75	28,04	40,98	12,53	12,94	5,82	-2,50	23,06
11,86	27,99	41,36	13,68	13,37	5,98	-2,23	24,66
12,00	28,01	40,59	11,46	12,58	6,03	-2,16	21,62
12,25	27,99	40,18	10,42	12,19	5,82	-1,62	18,95
12,50	28,05	39,48	8,87	11,43	6,18	0,55	15,99

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,06	42,33	17,10	17,27	3,58	-11,86	34,76
11,75	25,02	42,87	19,36	17,85	4,52	-13,27	36,32
11,86	25,10	42,99	19,91	17,89	4,54	-13,09	35,64
12,00	24,98	42,28	16,90	17,30	5,06	-9,00	33,16
12,25	25,09	42,24	16,75	17,15	4,30	-6,77	30,21
12,50	25,01	42,04	16,00	17,03	4,05	-7,01	28,20

Table 34 : HPA-2 #1 module. Synthesis of power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vd=30V, Id=450mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

HPA-2 #2, HPA-2 #3 and HPA-2 #4 modules have been tested with the same approach. Synthesis of the RF performances measured with CW signal are provided in the following tables.

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,06	42,35	17,18	16,29	4,89	-12,08	33,97
11,75	26,12	42,88	19,41	16,76	5,67	-5,50	35,45
11,86	26,01	42,95	19,72	16,94	5,47	-5,98	34,71
12,00	26,01	42,14	16,37	16,13	5,82	-1,78	31,34
12,25	25,97	42,31	17,02	16,34	4,80	-0,73	29,40
12,50	26,07	42,07	16,11	16,00	4,68	-2,12	27,00

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	28,00	41,62	14,52	13,62	5,30	-7,00	27,45
11,75	26,10	41,35	13,65	15,25	4,41	0,93	27,54
11,86	25,98	41,34	13,61	15,36	4,21	-1,52	26,94
12,00	26,07	40,74	11,86	14,67	4,40	1,79	24,62
12,25	25,98	40,34	10,81	14,36	4,09	1,69	21,47
12,50	25,94	39,76	9,46	13,82	4,10	3,35	18,40

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,01	42,38	17,30	17,37	4,02	-8,24	35,83
11,75	24,98	43,16	20,70	18,18	5,08	-9,88	38,83
11,86	25,07	43,32	21,48	18,25	4,93	-7,51	38,09
12,00	25,11	42,52	17,86	17,41	5,64	-1,17	34,84
12,25	25,09	42,81	19,10	17,72	4,88	-4,96	32,48
12,50	25,10	42,70	18,62	17,60	4,08	-2,31	30,66

Table 35 : HPA-2 #2 module. Synthesis of power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vd=30V, Id=450mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	27,01	41,91	15,52	14,90	5,44	-13,93	27,54
11,75	27,02	42,14	16,37	15,12	5,97	-9,21	26,83
11,86	27,02	42,26	16,83	15,24	5,78	-6,86	27,09
12,00	26,98	40,98	12,53	14,00	6,38	-7,89	20,66
12,25	27,09	41,34	13,61	14,25	5,61	-6,56	21,14
12,50	27,13	40,93	12,39	13,80	5,60	-6,16	18,62

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	28,04	41,16	13,06	13,12	5,64	-8,67	23,22
11,75	27,97	41,07	12,79	13,10	5,92	-5,99	21,41
11,86	27,96	41,22	13,24	13,26	5,66	-3,98	21,99
12,00	28,07	39,84	9,64	11,77	6,30	-4,95	15,98
12,25	27,94	40,07	10,16	12,13	5,60	-3,13	16,70
12,50	28,04	39,60	9,12	11,56	5,68	-0,63	14,63

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,06	42,08	16,14	17,02	4,06	-7,55	31,48
11,75	24,99	42,64	18,37	17,65	4,74	-7,63	32,56
11,86	25,12	42,74	18,79	17,62	4,73	-7,57	32,37
12,00	24,96	41,65	14,62	16,69	5,29	-1,36	26,76
12,25	25,12	42,03	15,96	16,91	4,26	-2,40	26,75
12,50	25,09	41,74	14,93	16,65	3,98	-3,89	23,85

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Table 36 : HPA-2 #3 module. Synthesis of power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vd=30V, Id=450mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,95	42,26	16,83	15,31	5,02	-12,55	33,07
11,75	27,00	42,80	19,05	15,80	5,90	-11,23	34,27
11,86	26,92	42,83	19,19	15,91	5,98	-10,33	33,54
12,00	27,01	42,11	16,26	15,10	6,53	-6,04	30,02
12,25	27,08	42,28	16,90	15,20	5,76	-5,91	28,69
12,50	27,18	42,42	17,46	15,24	5,36	-5,95	28,35

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	28,11	41,52	14,19	13,41	5,39	####	27,61
11,75	28,02	41,93	15,60	13,91	5,71	-5,30	28,49
11,86	28,03	41,97	15,74	13,94	5,78	-4,90	28,03
12,00	28,13	41,25	13,34	13,12	6,25	-4,16	24,60
12,25	28,13	41,17	13,09	13,04	5,60	-3,91	23,13
12,50	28,02	40,84	12,13	12,82	5,40	-2,20	21,26

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,98	42,28	16,90	16,30	3,60	-19,63	35,26
11,75	25,98	43,08	20,32	17,10	4,72	-19,64	38,13
11,86	26,08	43,14	20,61	17,06	5,17	-19,52	37,00
12,00	26,12	42,46	17,62	16,34	5,90	-10,67	33,86
12,25	26,05	42,66	18,45	16,61	5,03	-11,32	31,93
12,50	25,97	42,91	19,54	16,94	4,24	-10,68	32,18

Table 37 : HPA-2 #4 module. Synthesis of power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vd=30V, Id=450mA. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

3.7.1.3 *Multi-carrier mode power measurements.*

In the following part, multicarrier measurements are presented. 4x HPA modules have been tested with Vds=30V and Ids=450mA for biasing point fixed in small signal. Multi-carrier measurements have been performed at Temp=[-10°C, 25°C, 85°C]. Characteristics of the multicarrier signal applied are:

- Centre frequency=12GHz
- Span=1GHz
- Nb of carriers=3000
- Notch=1% centered at 12GHz

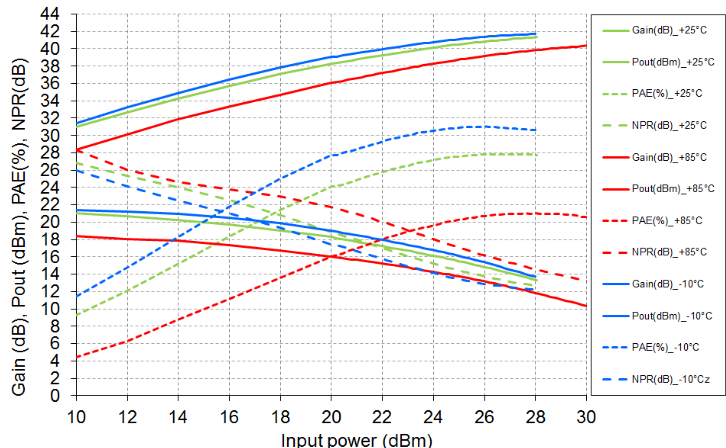

Figure 222 : HPA-2 #1 module. Power measurements with multi-carrier signal. Temp=[-10°C, 25°C, 85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch. Gain(dB), PAE(%), NPR(dB), Pout(dBm) vs Pin(dBm)

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In the following table are summarized the main parameters measured during multi-carrier measurements : Pout / NPR / PAE

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	15,05	24,22	40,20	10,48	15,99	27,25
	13,98	25,63	40,71	11,78	15,08	27,76
Temp=85°C	15,01	27,41	39,65	9,23	12,24	20,98
	14,03	28,79	40,06	10,13	11,27	20,95
Temp=-10°C	15,1	22,79	40,30	10,71	17,51	29,89
	13,99	23,01	40,84	12,12	16,65	30,66

Table 38 : HPA-2 #1 module. Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch

HPA-2 #2, HPA-2 #3 and HPA-2 #4 modules have been tested with the same approach. Synthesis of the RF performances measured with multi-carrier signal are provided in the following tables.

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	14,95	23,58	40,27	10,65	16,69	28,55
	13,99	24,81	40,74	11,86	15,93	29,11
Temp=85°C	14,99	26,59	39,70	9,34	13,11	21,91
	14,05	27,84	40,12	10,27	12,27	22,14
Temp=-10°C	15,05	21,63	40,06	10,13	18,43	30,57
	14,04	23,00	40,61	11,51	17,61	31,74

Table 39 : HPA-2 #2 module. Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch.

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	14,99	23,99	39,83	9,62	15,84	22,89
	13,98	25,39	40,33	10,79	14,94	23,37
Temp=85°C	14,96	26,79	39,24	8,40	12,46	17,90
	13,94	28,20	39,68	9,29	11,48	18,00
Temp=-10°C	15,08	22,01	39,78	9,51	17,77	24,96
	14,03	23,60	40,39	10,93	16,79	25,71

Table 40 : HPA-2 #3 module. Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch.

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	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	15	23,60	40,19	10,44	16,59	27,91
	13,99	25,01	40,70	11,74	15,69	28,50
Temp=85°C	15,04	26,21	39,78	9,51	13,57	22,83
	13,92	27,81	40,27	10,64	12,46	23,01
Temp=-10°C	15,03	21,97	40,07	10,15	18,09	30,33
	14,02	23,38	40,58	11,42	17,20	31,37

Table 41 : HPA-2 #4 module. Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch

3.7.1.4 RF step measurements with multi-carrier signal : reliability of GH25 technology

The goal of this reliability study is to define a Safe Operating Area through RF Multicarrier step stress (2 dB compression, 4 dB compression, 6 dB compression, 8 dB compression). For that, a dedicated multicarrier test bench have been developed. Initial Measurements, intermediate RF measurements, final measurements and in situ monitoring are performed during this evaluation. Test plan is provided in the following table:

	Function	HPA
	FONDERIE	UMS GH25
	Frequency	12 GHz
	DC Bias	Vd = 28 Id = 460mA (Id1 = 60 mA; Id2 = 400 mA)
DC Life test	Number of Sample	NA
	T° JUNCTION (Objective)	NA
	Electrical constraint	NA
	Duration	NA
RF Life test	Number of Sample	3 + 1
	T°	25°C
	DC Biases	Nominal DC biases
	Electrical Constraint	Multicarrier
		Step stress :
		2 weeks at 2dBc, 4 dBc, 6dBc and 8 dBc
	Monitoring	Gate, drain current, Input, output power
	Initial, Final & Intermediate Measurment	DC characteristics : Ids (Vds, Vgs) -> Ids=500 mA, Schottky Characteristic
		RF Characteristic : Pout, Gain, Id vs Pin Phase vs input power

Table 42 : Test plan for RF step stress measurements of Ku-Band GH25 HPA-2 module

3 samples have been tested during RF step stress with multicarrier signal:

- Sample n°2 = SN2
- Sample n°3 = SN3
- Sample n°1 = SN1 (control sample reference)

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Multi carrier signal is generated using white noise source. The « white noise » bandwidth is = 1GHz . Synoptic and photographs of the multi-carrier test bench are provided in the following figures.

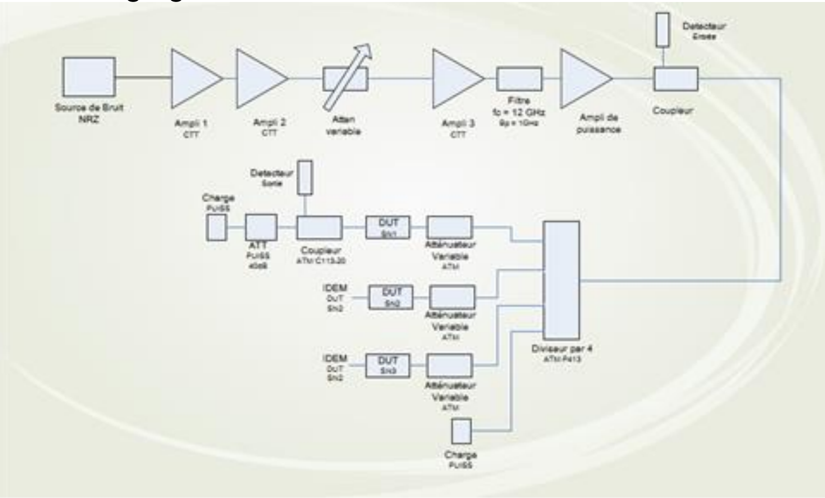

Figure 223 : Ku-Band Multi-carrier test bench

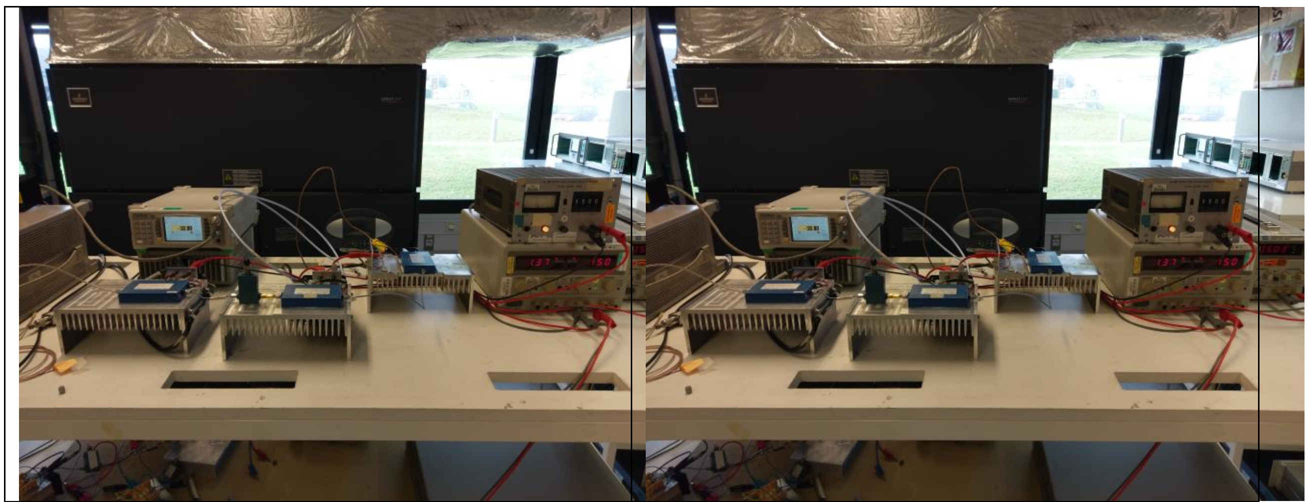

Figure 224 : Photographs of the Ku-Band multi-carrier test bench

The figure here above describes the signal level generated by the RF step stress test bench.

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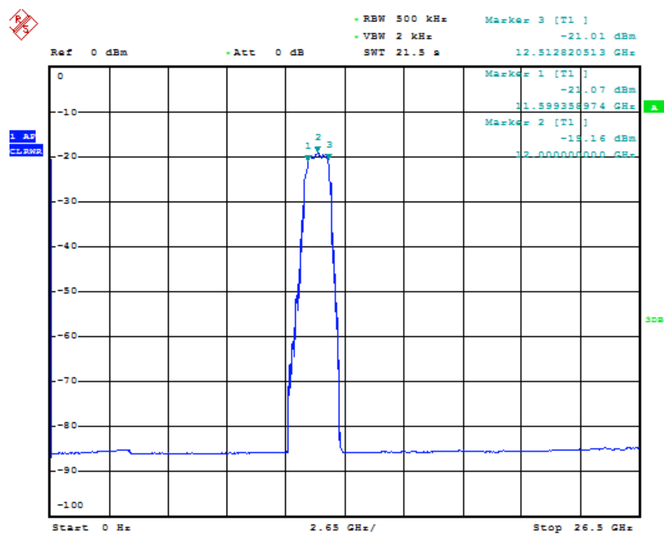

Figure 225 : Noise signal level at different point of the test bench

A dedicated test bench for initial, intermediate and final measurement bench is used for [S], AM/AM and AM/PM measurements after each step of compression (2 weeks / step from 4dBc to 8dBc). Synoptic and photographs of this test bench are provided in the following figures.

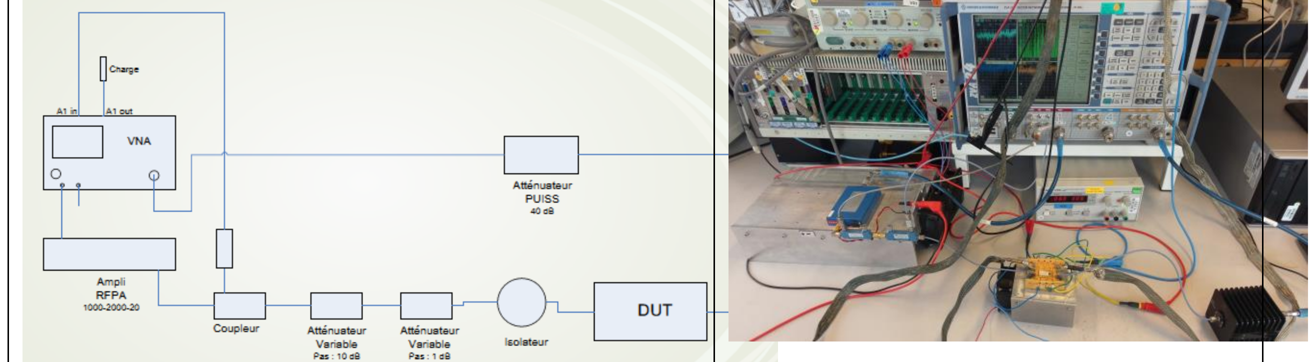

Figure 226 : Photography of the CW test bench for CW initial/intermediate and final measurements

Before starting the RF step stress campaign, initial characterization with the multicarrier signal have been performed in order to determine the non-linear characteristic of each samples.
In order to determine the power value during the in situ monitoring we use a detector. The power value versus the detected voltage is represented in the following graph.

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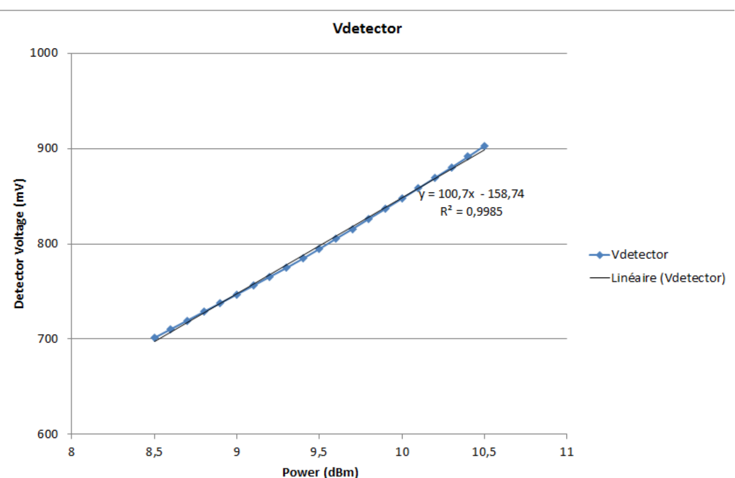

Figure 227 : Detector characterization : Detected voltage value (mV) versus power range(dBm)

On two HPA-2 modules (#2, #3), in Situ measurements have been continuously performed during steps @2dB, @4dB, 6dB, 8dB compression. The different parameters monitored are:

- Input power (dBm) and output power (dBm)
- Temperature (°C)
- Drain voltage (V) and Drain current (mA)
- Gate voltage (V) and gate current (mA)

An example of the in situ monitoring performed on HPA-2 module (#2) at Step 8dB compression is presented below:

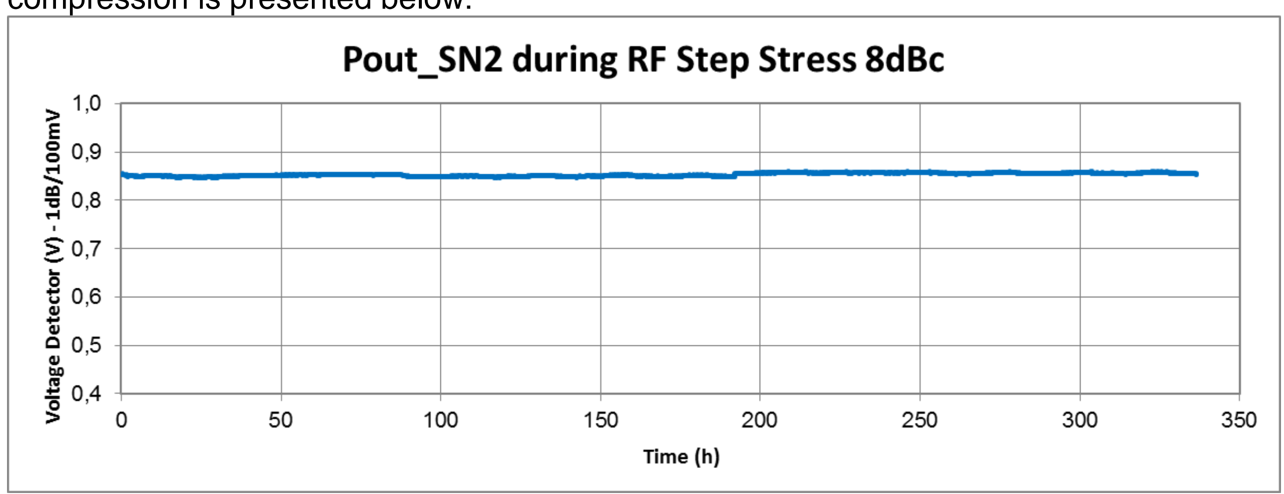

Figure 228 : HPA-2 module (#2). RF step stress measurement. Monitoring of Pout drift (detected voltage in V) during 8dBc compression step

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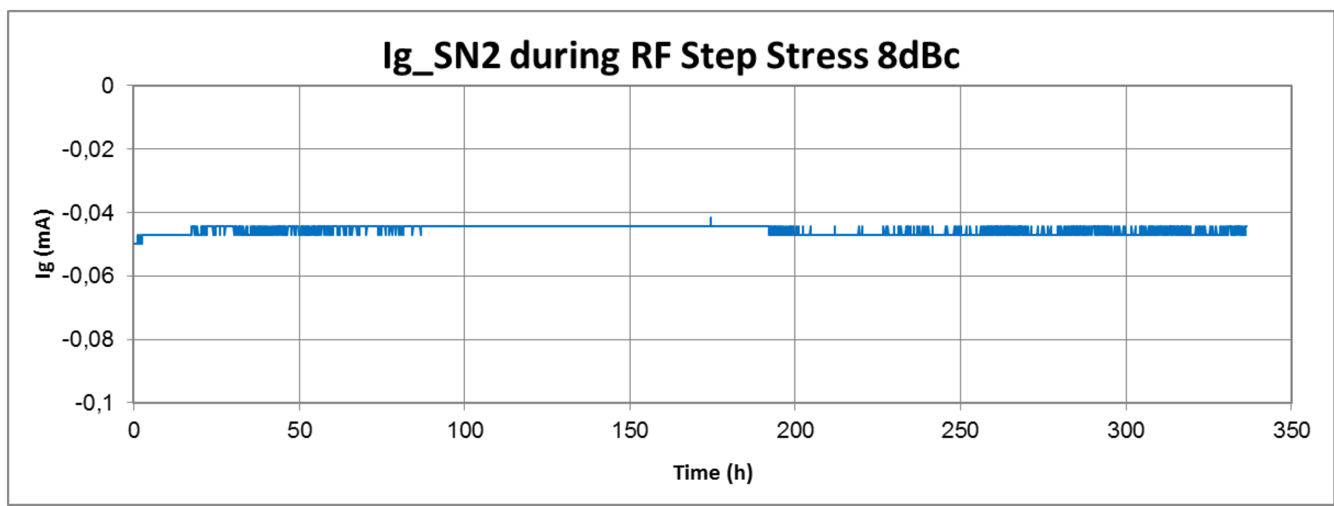
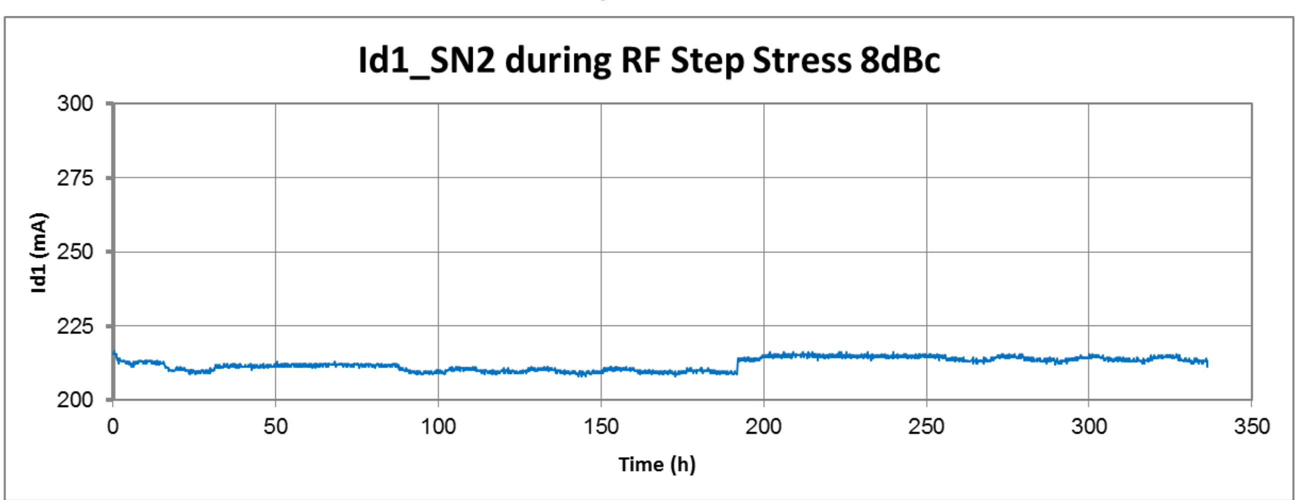


Figure 229 : HPA-2 module (#2). RF step stress measurement. Monitoring of Gate current drift during 8dBc compression step



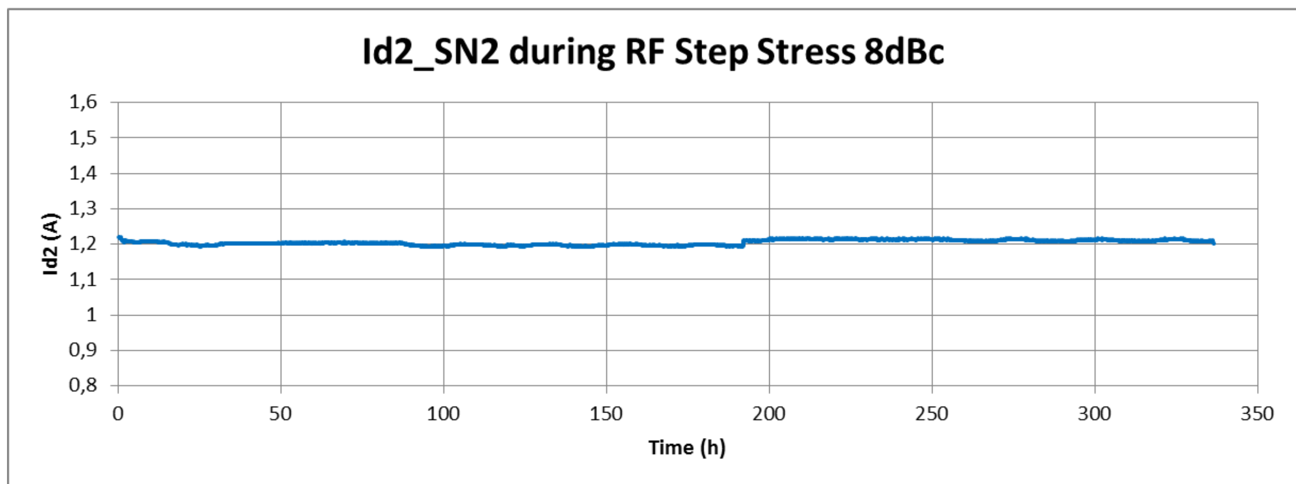


Figure 230 : HPA-2 module (#2). RF step stress measurement. Monitoring of Drain current drift during 8dBc compression step

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For each HPA-2 module (#2, #3) initial, intermediate and final have been performed. These measurements have consisted of:

- [S] parameters measurements
- CW characterizations (AMAM and AMPM)
- Static measurements

Measurement data are presented for HPA-2 module #2 in the following graphs.

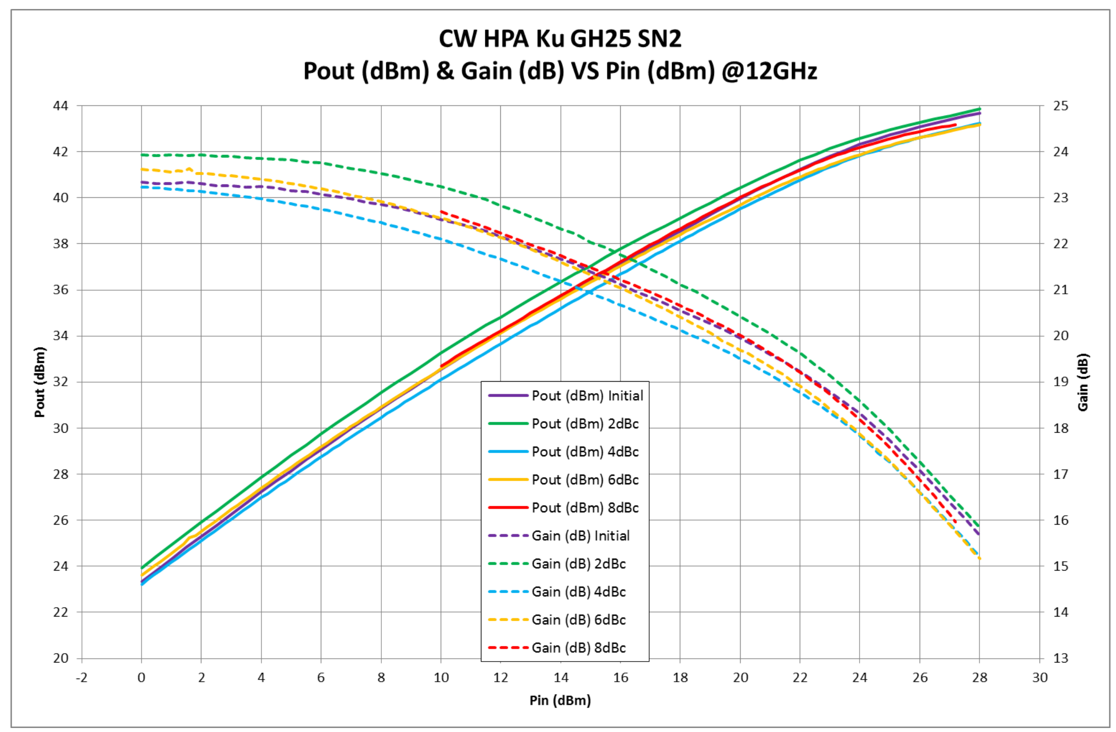

Figure 231 : HPA-2 module #2. AMAM characterization in CW mode after each compression step of the RF step stress measurements

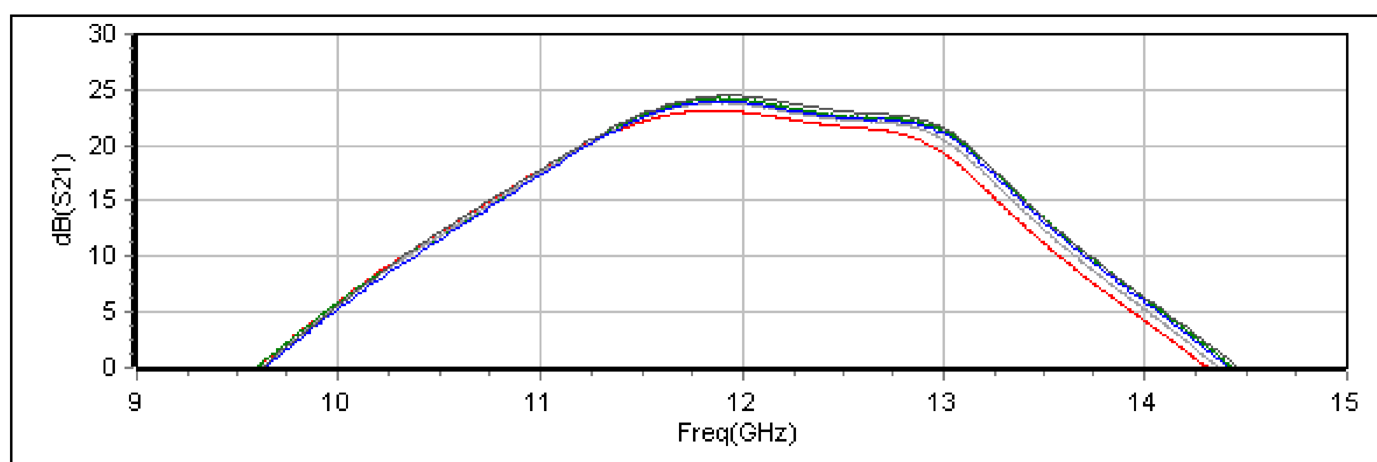

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Figure 232 : HPA-2 module #2. [S] parameters measurements after each compression step of the RF step stress measurements

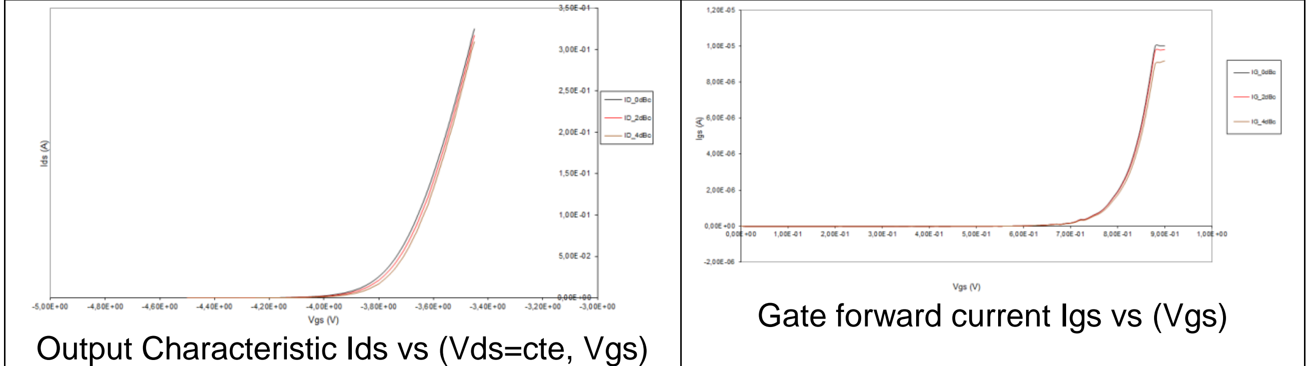

Figure 233 : HPA-2 module #2 Static measurements after each compression step of the RF step stress measurements

No significative drift have been pointed out during these stress steps. The drift observed on the 2 samples are also observed on the control sample.

In conclusion, TAS has performed during this evaluation, 2 kinds of measurements :

- In situ measurements (Pout, drain & gate current)
- Initial, intermediate (after each step) and final measurements :
  - CW (Pout vs Pin)
  - [S] measurements

During the monitoring no significant drifts have been observed.

3.7.2 MMIC Doherty HPA Modules test results

3.7.2.1 [S] Parameter measurements

On figure below the Doherty HPA module #1 (Full MMIC) S-parameters are given over a DC to 20GHz bandwidth with drain voltage of 30V and Ids_carrier=400mA (80mA/mm) and Ids_peaking=100mA (20mA/mm) fixed at Temp=25°C. This biasing point has been obtained during the multicarrier measurements and represent the best trade-off Pout/PAE/NPR. Measurements are performed versus Temp=[-10°C, 25°C, 85°C]

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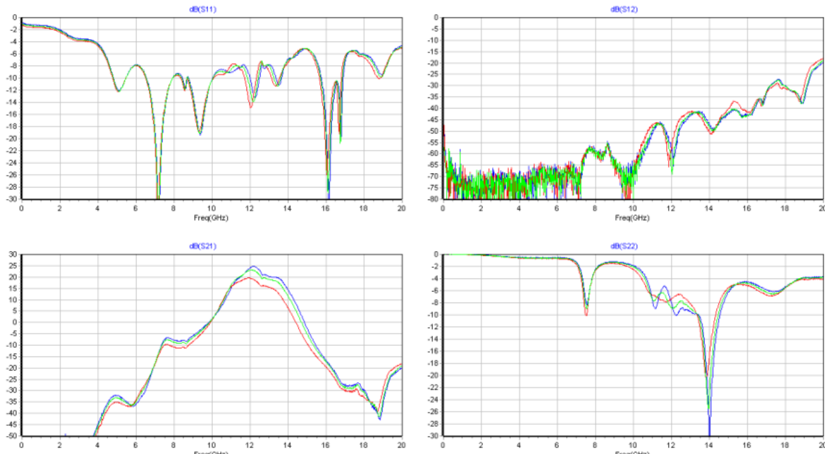

Figure 234 : MMIC Doherty HPA module #1 (Full MMIC). [S] parameters measurements. RF=[DC-20GHz], Vd=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C, Temp=[-10°C, 25°C, 85°C]

On the following figures, we focus on the Doherty HPA module #1 (Full MMIC) in-band frequency behavior. S21 variation is about 4dB between -10°C to 85°C at 12 GHz. At constant gate voltage current, the gain variation versus temperature is 0,21dB/°C

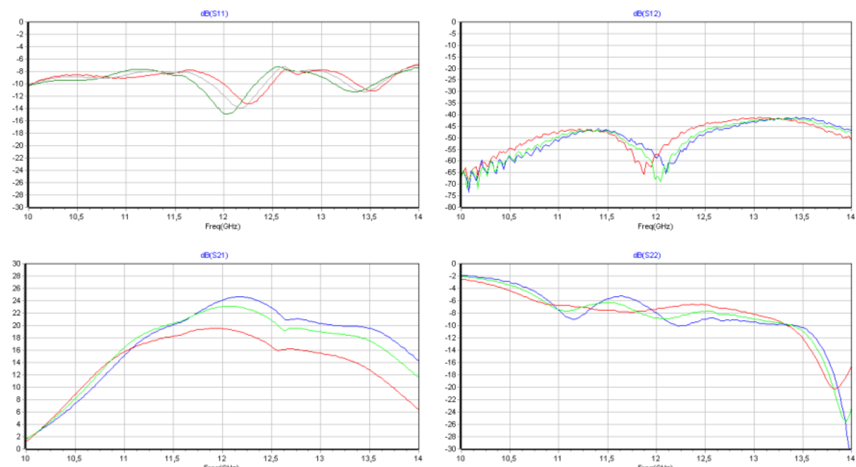

Figure 235 : MMIC Doherty HPA module #1 (Full MMIC). [S] parameters measurements. RF=[10-14GHz], Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C, Temp=[-10°C, 25°C, 85°C]

Hereafter, for three Doherty HPA modules (Full MMIC), the S-parameters are given over a DC to 20 GHz bandwidth with drain voltage of 30V and Ids_carrier=400mA (80mA/mm) and Ids_peaking=100mA (20mA/mm) fixed at Temp=25. Measurements are performed versus Temp=[-10°C, 25°C, 85°C]

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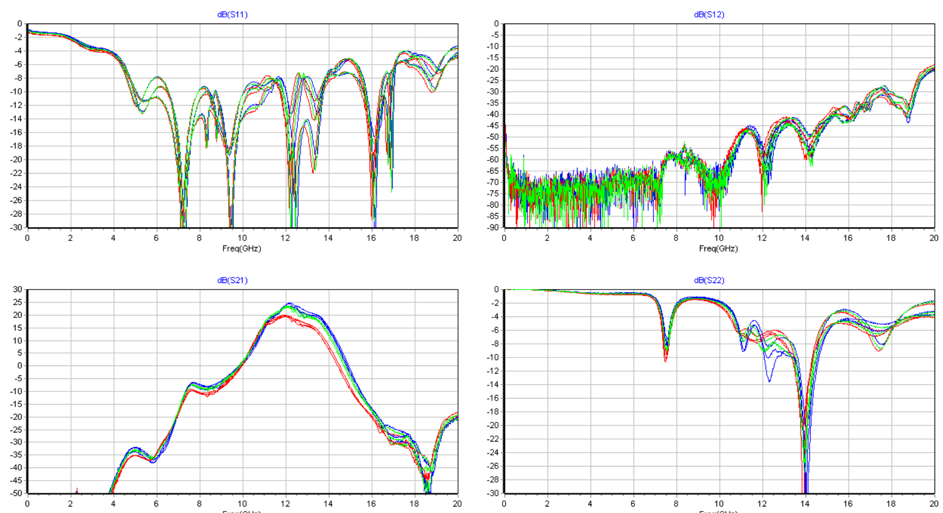

Figure 236 : 3x MMIC Doherty HPA module (Full MMIC). [S] parameters measurements. RF=[DC-20 GHz]. Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C, Temp=[-10°C, 25°C, 85°C]

On following figures, we focus on the Doherty HPA modules in-band frequency behavior. **Erreur ! Source du renvoi introuvable.** shows the dispersion on S11, S22 and S21 parameters versus HPA modules. Measurements are performed versus Temp=[-10°C, 25°C, 85°C]. Regarding S21 parameter, at 12 GHz, a maximum dispersion of 1dB is observed between the three HPA modules.

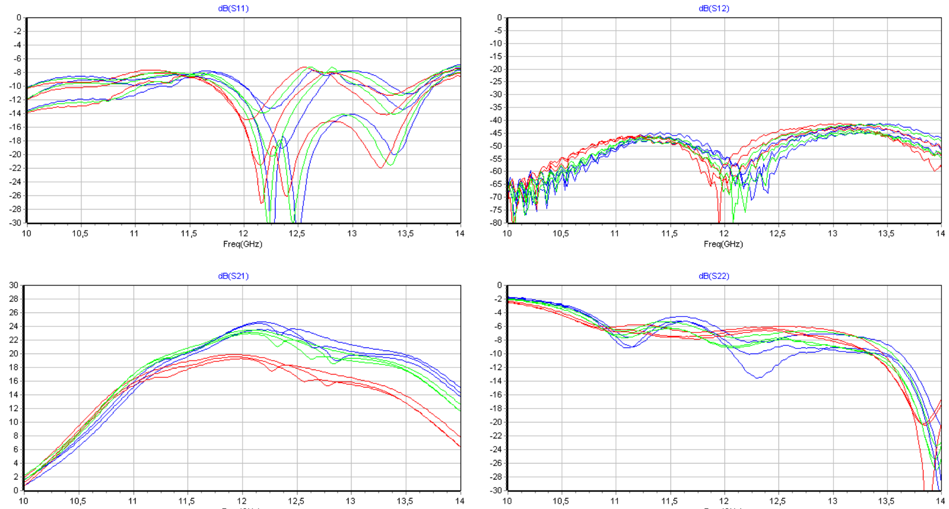

Figure 237 : 3x MMIC Doherty HPA module (Full MMIC). [S] parameters measurements. RF=[10-14 GHz]. Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C, Temp=[-10°C, 25°C, 85°C]

3.7.2.2 CW mode power measurements.

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The RF performances measured with a CW signal are presented in this chapter. The selected biasing point is: Vds=30V with Ids_carrier=400mA (80mA/mm) and Ids_peaking=100mA (20mA/mm). This biasing point is fixed at Temp=25°C. This biasing point has been obtained during the multicarrier measurements and represents the best trade-off Pout/PAE/NPR. The presented measurements are performed versus Temp=[-10°C, 25°C, 85°C].

The main RF performances obtained, output power, PAE, power gain and phase are presented below versus input power and different frequency points from [11.5GHz to 13GHz]. Measurements have been performed for Temp=[-10°C, 25°C, 85°C].

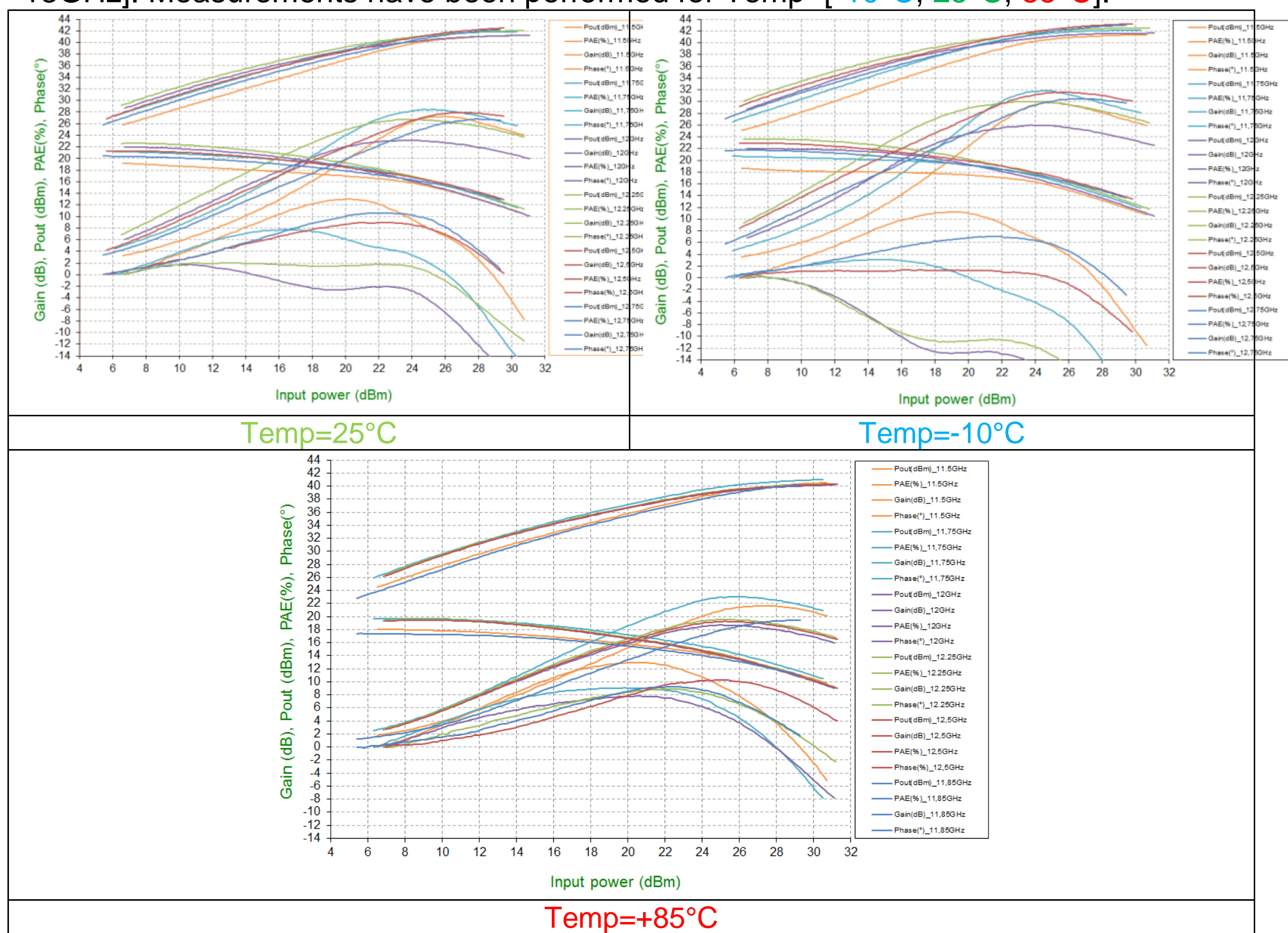

Figure 238 : MMIC Doherty HPA module#1 (Full MMIC). Power measurements with CW signal. Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C. Temp=[-10°C, 25°C, 85°C]. RF=[11,5 GHz to 13 GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

The results (Pout, Gain, PAE, Compression) are presented versus frequency and temperature. For each temperature, Pin has been fixed to obtain maximum of PAE.

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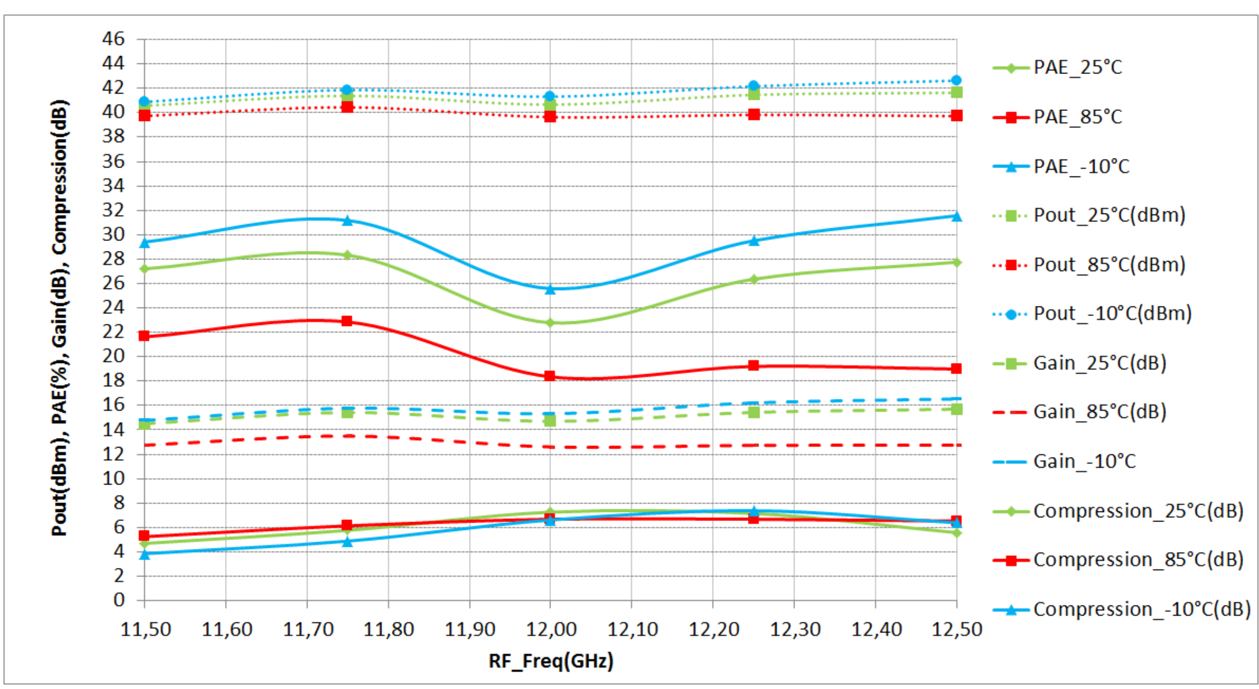

Figure 239 : MMIC Doherty HPA module#1 (Full MMIC). Power measurements with CW signal. Temp=[-10°C, 25°C, 85°C]. Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max.

Synthesis of the RF performances measured with CW signal are provided in the following table. Data are provided at PAE_max

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,07	40,58	11,43	14,51	4,70	6,51	27,21
11,75	25,96	41,39	13,77	15,43	5,77	0,33	28,33
12,00	25,96	40,67	11,67	14,71	7,26	-6,45	22,79
12,25	26,03	41,47	14,03	15,44	7,15	-1,08	26,36
12,50	25,94	41,64	14,59	15,70	5,58	7,01	27,76

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,99	39,74	9,42	12,75	5,25	5,94	21,63
11,75	26,95	40,45	11,09	13,50	6,14	2,54	22,85
12,00	27,03	39,64	9,20	12,61	6,68	1,82	18,36
12,25	27,09	39,83	9,62	12,74	6,68	5,17	19,21
12,50	26,98	39,73	9,40	12,75	6,53	9,55	18,99

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,11	40,89	12,27	14,78	3,86	3,55	29,41
11,75	26,09	41,87	15,38	15,78	4,89	-7,77	31,18
12,00	25,99	41,32	13,55	15,33	6,62	-19,28	25,59
12,25	25,95	42,17	16,48	16,22	7,38	-14,91	29,51
12,50	26,09	42,63	18,32	16,54	6,39	-1,29	31,56

Figure 240 : MMIC Doherty HPA module#1 (Full MMIC). Synthesis of power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

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Two other MMIC Doherty HPA modules have been tested with the same approach. Synthesis of the RF performances measured with CW signal are provided in the following tables.

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,08	40,51	11,25	15,43	4,51	1,03	27,27
11,75	25,08	41,29	13,46	16,21	5,62	-1,99	28,56
12,00	24,97	40,63	11,56	15,66	6,94	-3,85	23,24
12,25	24,98	41,42	13,87	16,44	6,57	2,25	26,75
12,50	25,02	41,84	15,28	16,82	5,16	7,68	28,57

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,08	39,66	9,25	13,58	5,01	1,38	21,87
11,75	26,08	40,30	10,72	14,22	5,70	1,60	23,05
12,00	26,09	39,58	9,08	13,49	6,18	3,25	18,75
12,25	26,14	40,16	10,38	14,02	5,52	5,53	21,40
12,50	26,01	40,19	10,45	14,18	4,49	7,84	21,77

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	23,97	40,60	11,48	16,63	3,47	3,64	29,68
11,75	23,95	41,47	14,03	17,52	4,61	-2,39	31,33
12,00	24,01	40,95	12,45	16,94	6,49	-8,04	25,88
12,25	24,10	41,85	15,31	17,75	6,86	-2,64	29,78
12,50	24,00	42,36	17,22	18,36	5,42	6,80	32,10

Figure 241 : MMIC Doherty HPA module#2 (Full MMIC). Synthesis of power measurements with CW signal. Temp=[-10°C, 25°C, 85°C], Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,00	40,13	10,30	14,13	5,16	6,69	24,96
11,75	25,97	40,99	12,56	15,02	6,01	-2,51	25,99
12,00	26,08	40,24	10,57	14,16	7,55	-6,57	20,23
12,25	25,96	41,05	12,74	15,09	6,81	-0,03	24,65
12,50	26,02	41,56	14,32	15,54	5,50	5,52	24,86

Figure 242 : MMIC Doherty HPA module#3 (Full MMIC). Synthesis of power measurements with CW signal. Vds=30V. Fixed Ids_carrier=400mA (80mA/mm) and Fixed Ids_peaking=100mA (20mA/mm) @25°C. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) @PAE_max

3.7.2.3 Multi-carrier mode power measurements.

The multicarrier signal characteristics is presented below:

- Centre frequency: 12GHz
- Bandwidth : 1GHz
- Number of carriers: 3000
- Notch: 1%
- Position of notch: centred at 12GHz

Performance of the Ku-Band Doherty HPA module (Full MMIC) has been optimized directly during the multicarrier measurements by tuning the biasing point of the peaking path and the carrier path.

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In the table below, the performance (Pout/PAE) for NPR=15dB and NPR=14dB are presented versus different biasing points:

- Drain current of the carrier path from 300mA (60mA/mm) to 700mA(140mA)
- Drain current of the peaking path from 0mA(0mA/mm) to 100mA(20mA/mm)

At NPR15	Gain	Pin	Pout	PAE	NPR
Data (500mA_100mA)	17.41	21.61	38.93	24.69	14.96
Data (400mA_100mA)	17.00	21.81	38.81	24.59	15.02
Data (500mA_150mA)	17.52	21.42	38.95	24.49	15.07
Data (500mA_5mA)	16.60	21.78	38.38	24.21	15.02
Data (600mA_100mA)	16.95	22.00	38.96	24.18	15.02
Data (300mA_5mA)	16.25	21.86	38.11	24.01	14.97
Data (500mA_0mA)	15.32	22.61	37.93	23.50	15.05
Data (700mA_5mA)	16.00	22.59	38.59	23.14	15.05

At NPR15	Gain	Pin	Pout	PAE	NPR
Data (500mA_100mA)	17.41	21.61	38.93	24.69	14.96
Data (400mA_100mA)	17.00	21.81	38.81	24.59	15.02
Data (500mA_150mA)	17.52	21.42	38.95	24.49	15.07
Data (500mA_5mA)	16.60	21.78	38.38	24.21	15.02
Data (600mA_100mA)	16.95	22.00	38.96	24.18	15.02
Data (300mA_5mA)	16.25	21.86	38.11	24.01	14.97
Data (500mA_0mA)	15.32	22.61	37.93	23.50	15.05
Data (700mA_5mA)	16.00	22.59	38.59	23.14	15.05

Figure 243 : MMIC Doherty HPA module#1 (Full MMIC). Optimization of the biasing point. Multi-carrier measurements. Temp=25°C

Best compromise is obtained for Ids_carrier=400mA and Ids_peaking=100mA corresponding to a minimum of AMPM variation vs Pin with CW signal. On figure below, multi-carrier measurements are given versus input power.

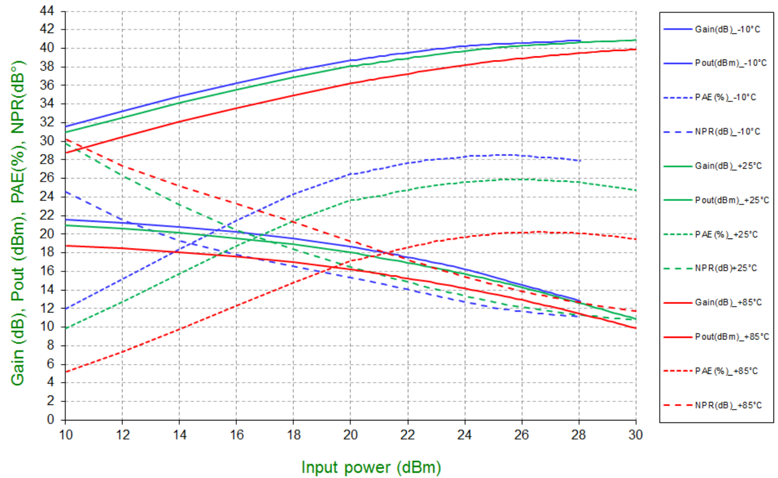

Figure 244 : Doherty HPA module#1 (Full MMIC). Power measurements with multi-carrier signal. Temp=[-10°C, 25°C, 85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch. Gain(dB), PAE(%), NPR(dB), Pout(dBm) vs Pin(dBm)

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In the following table are summarized the main parameters measured during multi-carrier measurements : Pout / NPR / PAE

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	15,05	21,77	38,84	7,66	17,07	24,63
	14,12	22,97	39,35	8,60	16,38	25,24
Temp=85°C	14,97	24,57	38,42	6,95	13,85	19,89
	14,02	25,80	38,87	7,70	13,06	20,18
Temp=-10°C	15	20,63	38,96	7,87	18,26	26,76
	14,08	21,98	39,54	8,99	17,56	27,62

Figure 245 : Doherty HPA module#1 (Full MMIC). Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch.

Two other MMIC Doherty HPA modules have been tested with the same approach. Synthesis of the RF performances measured with multicarrier signal are provided in the following tables.

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	15,06	20,99	38,83	7,64	17,84	24,74
	14,06	22,39	39,40	8,71	17,01	25,39
Temp=85°C	14,98	23,63	38,40	6,92	14,78	20,12
	13,97	25,05	38,92	7,80	13,88	20,45
Temp=-10°C	14,88	20,00	39,21	8,34	19,22	27,31
	14,02	21,41	39,73	9,40	18,33	27,79

Figure 246 : Doherty HPA module#2 (Full MMIC). Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch.

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	15,01	21,61	38,29	6,75	16,68	21,82
	14,06	22,98	38,84	7,65	15,86	22,34
Temp=85°C	15,07	24,40	38,02	6,33	13,62	17,89
	14,05	25,78	38,52	7,12	12,74	18,18
Temp=-10°C	14,98	21,19	38,89	7,75	17,71	24,83
	14,08	22,39	39,35	8,62	16,96	25,34

Figure 247 : Doherty HPA module#3 (Full MMIC). Synthesis of power measurements with multi-carrier signal. Temp=[-10°C, +25°C, +85°C]. Vds=30V, RF=12GHz, Span=1GHz, 3000 carriers, 1% notch.

3.7.2.4 Comparison results between HPA-2 module and MMIC Doherty HPA module

The table below, presents the comparison results between HPA-2 module and MMIC Doherty HPA module

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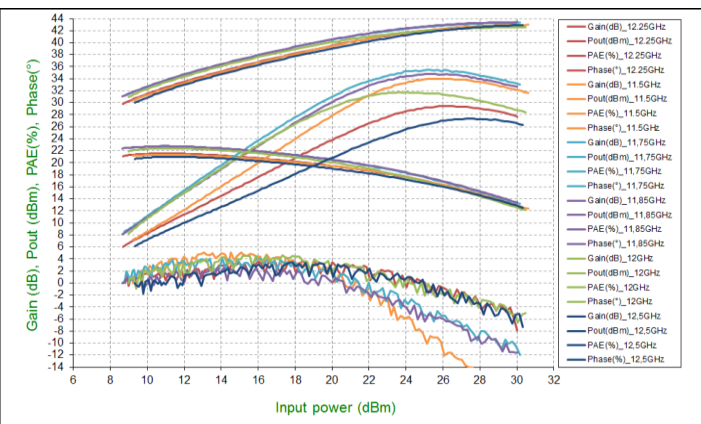

HPA-2 module. Power measurements with CW signal. Temp=25°C. RF=[11,5 GHz to 12.5 GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

MMIC Doherty HPA module (Full MMIC). Power measurements with CW signal. Temp=25°C. RF=[11,5 GHz to 12.5 GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs Pin(dBm)

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	26,06	42,35	17,18	16,29	4,89	-12,08	33,97
11,75	26,12	42,88	19,41	16,76	5,67	-5,50	35,45
11,86	26,01	42,95	19,72	16,94	5,47	-5,98	34,71
12,00	26,01	42,14	16,37	16,13	5,82	-1,78	31,34
12,25	25,97	42,31	17,02	16,34	4,80	-0,73	29,40
12,50	26,07	42,07	16,11	16,00	4,68	-2,12	27,00

HPA-2 module. Power measurements with CW signal. Temp=25°C. RF=[11,5 GHz to 13 GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) for PAE_max

Freq (GHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	Compression (dB)	Phase (°)	PAE (%)
11,50	25,08	40,51	11,25	15,43	4,51	1,03	27,27
11,75	25,08	41,29	13,46	16,21	5,62	-1,99	28,56
12,00	24,97	40,63	11,56	15,66	6,94	-3,85	23,24
12,25	24,98	41,42	13,87	16,44	6,57	2,25	26,75
12,50	25,02	41,84	15,28	16,82	5,16	7,68	28,57

MMIC Doherty HPA module (Full MMIC). Power measurements with CW signal. Temp=25°C. RF=[11,5 GHz to 13 GHz]. Gain(dB), PAE(%), Pout(dBm), Phase(deg) vs RFfreq(GHz) for PAE_max

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	14,95	23,58	40,27	10,65	16,69	28,55
	13,99	24,81	40,74	11,86	15,93	29,11
Temp=85°C	14,99	26,59	39,70	9,34	13,11	21,91
	14,05	27,84	40,12	10,27	12,27	22,14
Temp=-10°C	15,05	21,63	40,06	10,13	18,43	30,57
	14,04	23,00	40,61	11,51	17,61	31,74

HPA-2 module. Power measurements with multicarrier signal.

	NPR(dB)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	PAE(%)
Temp=25°C	15,06	20,99	38,83	7,64	17,84	24,74
	14,06	22,39	39,40	8,71	17,01	25,39
Temp=85°C	14,98	23,63	38,40	6,92	14,78	20,12
	13,97	25,05	38,92	7,80	13,88	20,45
Temp=-10°C	14,88	20,00	39,21	8,34	19,22	27,31
	14,02	21,41	39,73	9,40	18,33	27,79

MMIC Doherty HPA module. Power measurements with multicarrier signal.

Table 43 : Comparison results between HPA-2 module and MMIC Doherty HPA module

Based on the comparisons provided in the previous table, the preliminary conclusions on the development of a Large-band (1GHz bandwidth) and high power Ku-Band GH25 MMIC Doherty HPA module are:

- In CW mode:
  - Maximum of PAE for Doherty architecture is lower than the PAE obtained with a classical Class AB architecture
  - The Pout associated to the PAE_max is lower for Doherty architecture
  - AMPM vs Pin and frequency bandwidth is much more important for Doherty architecture

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- In Multicarrier-mode (NPR=14dB and NPR=15dB), PAE and Pout for PAE are lower for Doherty architecture

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4. CRITICAL ASSESEMENT OF HPA MODULE

4.1 L-band applications: comparison of SSPA using GaN HPA-1 module with a conventional GaAs flat mounted SSPA and TWTA

A Trade-Off between solutions with LTWTA and SSPA has been conducted. Results are presented in the following table. For the new generation of payload, a L-band GaN SSPA solution using HPA-1 module developed in this study and improved thermal management solutions brings many benefits, compared to a LTWTA solution and to a conventional GaAs SSPA, in term of:

- Improved electrical performances with multi-carrier signal
- Mass reduction
- Footprint reduction
- Higher operating temperature
- Simplified implementation during payload integration

	Solution with L-band TWT	Solution with L-band SSPA	
	TWTA	GaAs SSPA with standard housing and 2x GaAs HPA modules in RF chain	GaN SSPA with vertical housing and single GaN HPA-1 module in RF chain
RF performances with CW signal	Pout=43W PAE=57% (at 65°C)	Pout=43W PAE=45% (at 65°C)	Pout=50W PAE=58% (at 85°C)
RF performances with multi-carrier signal	Pout=25W PAE=45% @NPR=14dB (at 85°C)	Pout=25W PAE=36% @NPR=14dB (65°C)	Pout=32W PAE=45,5% @NPR=14dB (Temp=85°C)
Mass	4340g	1300g	1439g
Temperature	2 zones: 65°C (CAMP) 85°C (TWT)	Single zone: 65°C	Single zone: 85°C
Footprint	5 box: CAMP + TWT + EPC + Circulator + Load + (DC cable + RF cable)	Single box: 250x123mm²	Single box: 240x105mm²
	7,1dm²	3,1dm²	2,5dm²
Payload Integration complexity	Reference	++	+++

Table 44 : Trade-Off GaAs SSPA vs GaN SSPA (using HPA-1 module) vs TWTA

The target market is composed of the historical MSS market, the FSS and data relay satellite
market, the high power SSPA market.

- Mobile Satellite Service (MSS) Market: even if the MSS market cannot be considered as a steady market, there are regular opportunities for replacement satellites in existing constellations such as Inmarsat, Thuraya. It is forecast that one such replacement satellite will be ordered each year. Each satellite includes a large number of SSPA's (typically 100). We have conservatively figured a commercial success rate in this market of 50%, hence the number of 50/year on average.

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- Fixed Service Satellite (FSS) & Data Relay Satellite Market: there is also a number of opportunities in L- and S-band in this market,. The number of SSPA's per payload is smaller (in the order of 4 to 10 per satellite) and the number of opportunities estimated at 1 per year.
- High power SSPA market: beyond the proposed 50W SSPA, further developments in higher power (by e.g. paralleling output HPA's) will be able to address the higher-power L-band SSPA market for navigation repeaters (WAAS, EGNOS) which is also relatively steady at 1 payload per year with 4 SSPA's each.

4.2 Ku-band applications: comparison of SSPA using GaN HPA-2 module with a LC-TWTA equipment.

Based on HPA-2 module developed in the frame of this study, a trade-off has been performed achieved by TAS-F on a LC-SSPA.

This trade-off, presented in the following table, shows that a Ku-Band LC-SSPA using a current commercial European 0.25µm GaN technology (GH25 from UMS) and a low loss space combiner technique for output power section was not able to compete with a Ku-Band LC-TWTA solution regarding the electrical performance: LC-TWTA PAE was 30 points higher than the LC-SSPA one at saturation. If this gap was reduced down to 24 points in multi-carrier mode, the comparison remained clearly at LC-SSPA disadvantage.

It is then clear that a GH25 based LC-SSPA would present insufficient electric performances (low PAE and reduced frequency bandwidth) and that a technological breakthrough is required to increase this performance (Pout/PAE/NPR/Instantaneous frequency bandwidth).

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		Ku-band Linearized Equipment	
		Solution with TWT	Solution with SSPA
		Dual Ku-band LC-TWTA	1x RF GH25 160W power section (8x 20W MMIC PA with space combiner)
Mechanical caracteristics	Equipment's display		
	Technology for RF chain	GaAs for low level RF chain(LDLA) TWT for power section	GaAs for low level RF chain(LDLA) UMS GH25 for RF power section
	Architecture's description for 1x RF chain:	Assembly of 4 box 1x TWTs + Dual LC-EPC + 1x Circulator + 1x Load DC and RF cables: + 1x High Power DC cables (LC-EPC to TWT) + 1x RF cables (LC-EPC to TWT) + 2x High Power RF cables (TWT to circulator and circulator to load)	Stand-alone (1x box) including: + 1x RF power GaN section (8x HPA) + EPC / TMTC board + Low level RF chain (LDLA) + HPI
	Temperature	2 areas: 65°C (LC-EPC) 85°C (TWT)	1 area: 75°C and 85°C
	Mass for single RF chain	2800g	2300g
	Footprint for single RF chain	4,5dm²	3,4dm²
Functions	LDLA functions	Yes	Yes
	Power Flexibility	No	Yes
Performance	Frequency Bandwidth	1GHz	0,5 GHz (up to 1GHz to be confirmed by measurements)
Performance with Multi-carrier Signal	NPR	15dB	15dB
	Pout	95W	95W
	PAE	46,0%	22%
Performance with CW Signal	Pout	175W	175W
	PAE	61%	30%

Table 45 : Current comparison between Ku-Band a LC-TWTA and a LC-SSPA based on the GH25 GaN technology associated to the space combiner technique

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