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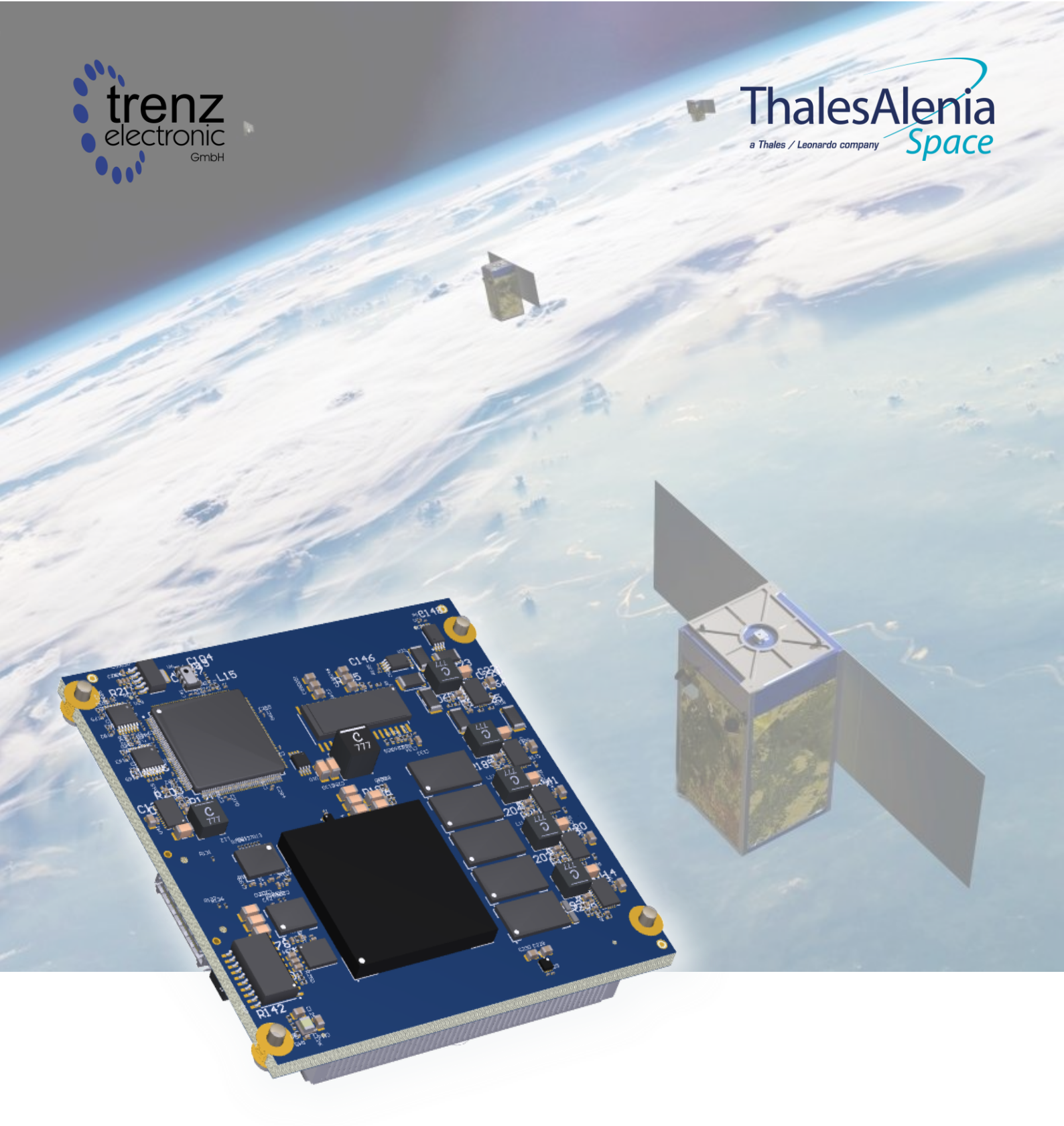


multiMIND payload processing core

high performance processing system for nanosat SDR / EO payloads

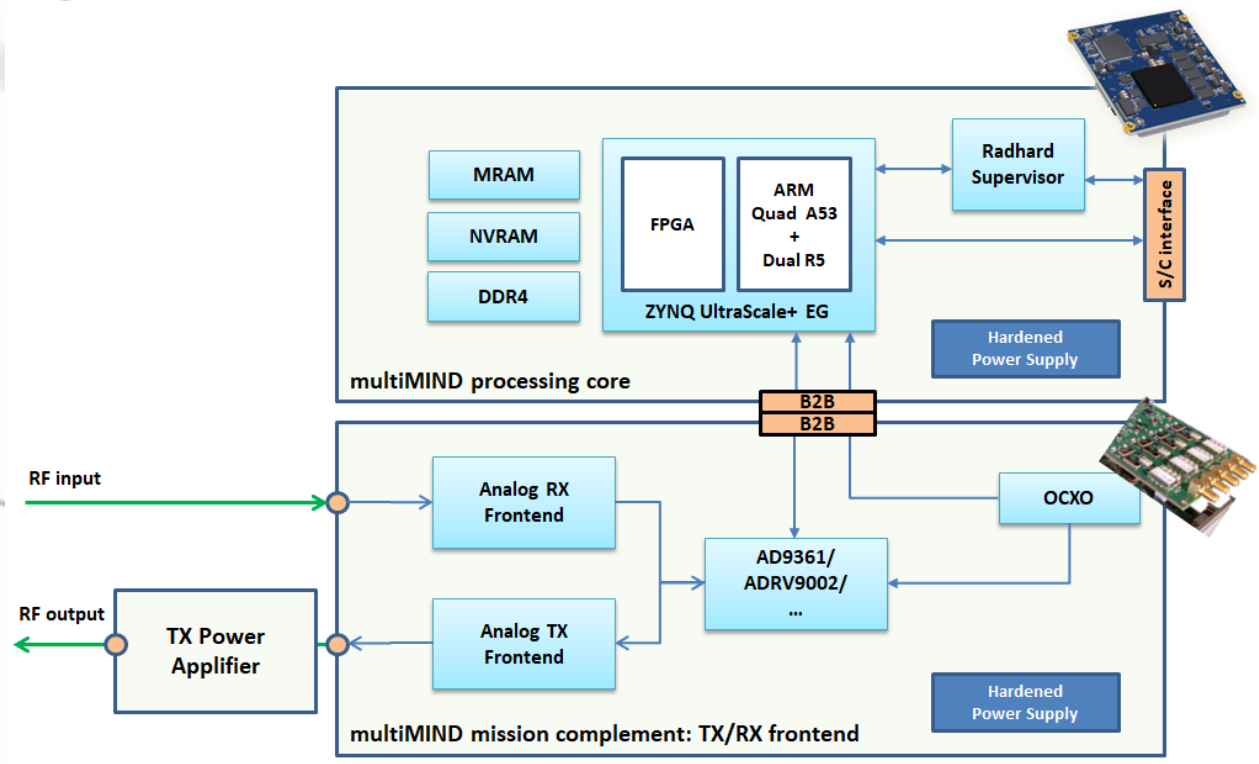
V1.12

COTS-based multi-mission signal processing system

Smaller, less power but more performance – this is the trend for current micro-satellites. Signal and image processing missions have a continuously increasing demand of on-board processing. To answer this need, Thales Alenia Space Germany and Trenz Electronic have joined their expertise to design and offer a robust and efficient solution employing latest-generation COTS multi-core processing systems with FPGA fabric in one single chip (MPSoC).

The **multiMIND** solution is a generic, cubesat-ready component to be used as central processing and SDR (Software Defined Radio) core for a variety of applications such as IoT/M2M, ADS-B, AIS, VDES / VHF COM, spectrum monitoring, signal intelligence and earth observation. The underlying approach is to implement generic, complex elements in one standard product, which is prepared to easily accept mission specific complements (RF-frontends, specific interface boards etc.). multiMIND uses the Xilinx UltraScale+ family as successor of the well-known Zynq 7000 series, but with even higher performance and less power consumption. Safe operation on LEO satellites is ensured by SEE robust design and optional innovative radiation shielding.

A true rad-hard supervisor detects and mitigates critical SEE ensuring survival of the system even in adverse radiation environment. Vital interfaces to the satellite platform are managed by this device and consequently remain available continuously. This allows the use of further COTS elements, including non-rad hard VHDL IP cores or standard operating systems like Linux – shortening dramatically mission specific firmware and software development time. The supervisor operates independently and ensures always the return to a defined and safe state.



Exemplary SDR payload architecture using multiMIND as processing core

The MPSoC core stores multiple configurations which can be dynamically loaded in flight. Upload of new FPGA bitstream or application S/W is possible in orbit.

A generic high speed interface connects custom and specific mission boards enabling a variety of missions and applications. State-of-the-art drivers allow use of latest-generation peripherals also in the RF stage.

multiMIND Characteristics

Item	Value	Remark
System Operation		
MPSoC family	ZU{6, 9, 15}EG	Xilinx Zynq UltraScale +; fabric size depends on mission specific requirements
Watchdog / Supervisor	M4	Rad hard Arm Core @ 100 MHz
MPSoC Processor Cores	Quad A53 + Dual R5	A53 @ 1.5 GHz, R5 @ 600 MHz
Embedded Logic (LUT)	215K .. 341K	Same as Kintex UltraScale+
Working memory	4 GByte	Connected to MPSoC Processing System
Signal processing memory	via PS	Via shared PS memory access by PL
NV Memory	2∗128 MByte + 512 kByte	NOR flashes for code / bitstream + MRAM for config
NV mass memory	2 ∗ 16 GByte	eMMC NAND flash (SLC mode) with file system
O/S (MPSoC ARM)	adapted Linux	e.g. Kubos, yoctoLinux, PetaLinux (BSP provided)
O/S (Supervisor)	Free RTOS	BSP / RefDesign provided
Environment		
System Design Lifetime	3 – 5 years	For LEO, max 600 km
Radiation (MPSoC / COTS)	10 krad (@ 4 mm Al)	Plus additional advanced spot shielding
Radiation (radhard watchdog)	300 krad (Si)	Latch-up immune for LET <= 110MeV-cm2 / mg, SEU protected with EDAC and memory scrubbing engine
Qualification Levels	ISO 19863	
SWaP - Size, Weight and Power		
PCB Size	Cubesat (9 * 9 cm²)	Cubesat form factor
Volume	< 0.5 U w. mezzanine card	Dedicated hi-density connectors; no PC104
Cooling concept	Heat spreader to side wall	No heat pipe; heat spreader acts as rad shield
Supply Voltage	NRB, 8 – 28V (5V optional)	No galvanic separation from bus
Power Consumption	< 5 .. 12W	Smallest .. largest variant (ZU6EG .. ZU15EG)
Standby Power	< 1000 mW	Standby (watchdog only, others OFF)
Communication Interfaces (via Mission Board)		
… to digitizing stages (mezzanine cards)	Serdes (JESD204B 12 Gbit/s) I²C/ SPI / ADC / GPIO	configurable within FPGA (FMC signals)
… to satellite bus	UART / CAN / Eth / GPIO / Clk	OBC, TC/HK via watchdog, mission data via MPSoC
… to slave modules	SPI, I²C, ADC, GPIO, Clk	Via mission board
… for debugging	JTAG, Ethernet, UART	JTAG, Ethernet, via dedicated debug adapter

Please Contact Thales Alenia Space Deutschland for the latest revision of this datasheet and for an individual proposal adapted to your mission's/payload's need:

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multiMIND Design Features and Overview

Main multiMIND design highlights

- Power distribution is solely made of latch-immune parts.
- Power stage and mission board accept direct supply from the cubesat NRB between 8 and 28 V. Optional, a direct 5V (regulated) feed is possible.
- Current monitoring of all lanes for latch-up mitigation.
- The boot memory holds at least 3 SoC configuration images:
    1. Golden image for backup usage,
    2. The current image,
    3. An update image also writeable by the supervisor.
- The non-volatile memory is protected by high-side switches for safe deactivation and therefore reducing the risk of SEE.
- Redundant NV memory for mission data allows the loss of one chip without performance penalties.
- The mission board connector is compatible to FMC HPC. This allows the use of standard FMC cards in the lab following a 'test-as-you-fly' approach.
- All PHYs needed for communication with the satellite bus are placed on a satellite bus interface board to allow specific adaptation.

The performance advantage available in COTS parts is the main driver for their usage. Rad-hard parts like Brave NGLarge from NanoExplore or SmartFusion2 from Microsemi cannot compete with the performance of current commercial MPSoCs. Seeing the need of a reliable usage of COTS parts, multiMIND consists out of 2 functional domains:

1. Non-vital functions:
    - High computational power needed,
    - Has to survive SEE, but short outages (resets) are acceptable.
2. Essential functions:
    - Low resource usage,
    - Outage-free operation required.

Non-vital functions can benefit from the performance of COTS hardware as well as COTS software and firmware in the COTS island. Essential functions are implemented using rad-hard space components.

Rad-hard parts that are immune to typical SEL, SEB and SEGR are used for the entire power conditioning of the numerous power rails needed for the MPSoC and other COTS parts on the PCB. This is a critical element especially as high currents and voltage stability are needed for the MPSoCs. Current and voltage is monitored to detect an operation beyond predefined limits. SEL are cleared by a cut-off of the current. COTS parts will be secured by high-side switches to securely isolate them from the current source. The reaction time of this power cut-off is critical to prevent permanent damage of a part.

Concerning non-destructive SEE, the following countermeasures are implemented:

- The configuration memory of the MPSoC PL is scrubbed. Well known blocks for this function are available.
- The rad-hard microcontroller acts as a watchdog for the MPSoC. The watchdog will command a (partial) reset in case parts of the MPSoC are not reacting, potentially due to a SEFI.
- Memory ECC is used widely. This is either done be built-in ECC or done manually.
- Multiple bit upsets (MBUs) make the need of spreading the data over several parts of each memory. This is covered by the architecture of Xilinx ZU+ MPSoCs.

The approach to use COTS in space in order to boost performance and reduce development costs is not limited to the hardware. Since firmware and software are vital elements and consume most development effort, the use of COTS blocks, operating system, routines and libraries becomes a crucial enabler.

Usually, COTS blocks are not primarily designed for use in space and do not have any mechanisms being tolerant to radiation effects. Exception handling in such routines might be not available or poor. Due to the separate watchdog concept, a full COTS based design can be used which will be supervised and reset when required.